EXC-1553PCI/MCH
EXC-1553cPCI/MCH

MIL-STD-1553
Test And Simulation Board For PCI Systems

User's Manual

EXCALIBUR SYSTEMS

311 Meacham Avenue ◆ Elmont ◆ NY 11003 ◆ Tel. (516) 327-0000 ◆ Fax (516) 327-4645
e-mail: excalibur@mil-1553.com website: www.mil-1553.com

Table of Contents

1 Introduction

1.1 Overview 1-1
1.2 Installation 1-4
1.2.1 Installing the Board 1-4
1.2.2 Adding Excalibur Software Tools. 1-4
1.3 1553 Bus Connections. 1-5
1.4 Note About Pointer Registers. 1-7
1.5 Technical Support 1-7

2 PCI Architecture

2.1 Memory Structure. 2-1
2.2 PCI Configuration Space Header. 2-2
2.3 PCI Configuration Registers. 2-3
2.3.1 Vendor Identification Register (VID) 2-3
2.3.2 Device Identification Register (DID) 2-3
2.3.3 PCI Command Register (PCICMD). 2-3
2.3.4 PCI Status Register (PCISTS). 2-4
2.3.5 Revision Identification Register (RID) 2-4
2.3.6 Class Code Register (CLCD) 2-5
2.3.7 Cache Line Register Size Register (CALN). 2-5
2.3.8 Latency Timer Register (LAT) 2-5
2.3.9 Header Type Register (HDR). 2-5
2.3.10 Built-In Self-Test Register (BIST) 2-5
2.3.11 Base Address Registers (BADR). 2-6
2.3.12 Cardbus CIS Pointer 2-6
2.3.13 Subsystem ID 2-7
2.3.14 Subvendor ID. 2-7
2.3.15 Expansion ROM Base Address Register (XROM) 2-7
2.3.16 Reserved 2-7
2.3.17 Interrupt Line Register (INTLN) 2-7
2.3.18 Interrupt Pin Register (INTPIN) 2-8
2.3.19 Minimum Grant Register (MINGNT) 2-8
2.3.20 Maximum Latency Register (MAXLAT) 2-8
2.4 Channel Memory Space. 2-9
2.4.1 Channel External Timer Clock Register 2-11
2.4.2 Channel Reset Register 2-11
2.5 Global Registers Map. 2-12
2.5.1 Board Identification Register 2-12
2.5.2 Software Reset Register 2-13
2.5.3 Interrupt Status Register 2-13
2.5.4 Interrupt Reset Register 2-13
2.5.5 Channel Info Registers 2-14
2.5.6 External Timer Clock Source Register 2-14

3 Bus Controller Operation

3.1 Bus Controller Message Processing 3-2
3.2 Control Registers: BC Mode 3-3
3.2.1 Control Register 3-4
3.2.2 Operational Status Register 3-5
3.2.3 Current Command Register 3-6
3.2.4 Interrupt Mask Register 3-6
3.2.5 Pending Interrupt Register 3-7
3.2.6 Interrupt Log List Pointer Register 3-8
3.2.7 BIT Word Register 3-8
3.2.8 Minor Frame Time Register 3-9
3.2.9 Command Block Pointer Register 3-9
3.3 BC Architecture 3-10
3.3.1 Control Word 3-11
3.3.2 1553 Command Words 3-14
3.3.3 Data Pointer 3-15
3.3.4 1553 Status Words 3-15
3.3.5 Branch Address 3-15
3.3.6 Timer Value 3-15
3.4 Command Block Chaining 3-16
3.5 Memory Architecture 3-17
3.6 MIL-STD-1553A/B Operation: BC Mode 3-18

4 Remote Terminal Operation

4.1 Control Registers 4-2
4.1.1 Control Register 4-3
4.1.2 Operational Status Register 4-5
4.1.3 Current Command Block Register 4-6
4.1.4 Interrupt Mask Register 4-6
4.1.5 Pending Interrupt Register 4-7
4.1.6 Interrupt Log List Pointer Register 4-8
4.1.7 BIT Word Register 4-8
4.1.8 Time Tag Register 4-9
4.1.9 RT Descriptor Pointer Register 4-9
4.1.10 1553 Status Word Bits Register 4-10
4.1.11 Illegalization Registers 4-11
4.2 Descriptor Block 4-13
4.2.1 Receive Control Word 4-15
4.2.2 Transmit Control Word 4-16
4.2.3 Mode Code Receive Control Word 4-17
4.2.4 Mode Code Transmit Control Word 4-18
4.2.5 Data Pointer A and B (Mode #0) 4-19
4.2.6 Ping-pong Handshake (Mode #0) 4-21
4.2.7 Broadcast Data Pointer (Mode #0) 4-22
4.3 Data Structures 4-23
4.3.1 Subaddress Receive Data 4-23
4.3.2 Subbaddress Transmit Data 4-24
4.3.3 Mode Code Data 4-25

4.4 RT Circular Buffer Modes 4-27
4.4.1 Mode #1 Operation 4-27
4.4.2 Mode #2 Operation 4-30
4.5 Mode Code and Subaddress 4-33
4.6 Encoder and Decoder 4-35
4.7 RT-to-RT Transfer Compare 4-36
4.8 Terminal Address 4-36
4.9 Reset 4-36
4.10 MIL-STD-1553A/B Operation: RT Mode 4-37

5 Bus Monitor Operation

5.1 Bus Monitor Message Processing 5-2
5.1.1 Error Condition Message Processing 5-2
5.1 Control Registers: BM Mode 5-3
5.1.1 Control Register 5-4
5.1.2 Operational Status Register 5-5
5.1.3 Current Command Register 5-6
5.1.4 Interrupt Mask Register 5-6
5.1.5 Pending Interrupt Register 5-7
5.1.6 Interrupt Log List Pointer Register 5-7
5.1.7 BIT Word Register 5-8
5.1.8 Time Tag Register 5-8
5.1.9 Initial Monitor Block Pointer Register 5-9
5.1.10 Initial Monitor Data Pointer Register 5-9
5.1.11 Monitor Block Counter Register 5-9
5.1.12 Monitor Filter Hi Register 5-10
5.1.13 Monitor Filter Lo Register 5-10
5.1 Bus Monitor Architecture 5-11
5.1.1 Message Information Word 5-11
5.1.2 Command Words 5-12
5.1.3 Data Pointer 5-12
5.1.4 Status Words 5-13
5.1.5 Time Tag 5-13
5.1.6 Reserved 5-13
5.1 Bus Monitor Block Chaining 5-13
5.1 Memory Architecture 5-14
5.1 RT/Concurrent Monitor Operation 5-15
5.1 MIL-STD-1553A/B Operation: BM Mode 5-16

6 Channel Interrupt Architecture

6.1 Overview 6-1
6.1.1 Interrupt Identification Word (IIW) 6-2
6.1.2 Interrupt Address Word (IAW) 6-2
6.1.3 Interrupt Log List Address 6-3

7 Mechanical And Electrical Specifications

7.1 Board Layout 7-2
7.1.1 *EXC-1553PCI/MCH* Board Layout 7-2
7.1.2 EXC-1553cPCI/MCH Board Layout. 7-3
7.2 LED Indicators 7-4
7.2.1 *EXC-1553PCI/MCH* LED Indicators 7-4
7.2.2 EXC-1553cPCI/MCH LED Indicators 7-4
7.3 DIP Switches 7-4
7.3.1 Selected ID DIP Switch [SW1]. 7-4
7.3.2 Multiple Board Applications 7-5
7.4 Jumpers 7-6
7.4.1 Channel 0 – Channel 3 1553 Coupling Mode Select Jumpers [JP2–JP17] 7-6
7.4.2 Factory Default Jumper Settings 7-6
7.5 Connectors. 7-7
7.5.1 Connector J1 Pinouts 7-8
7.5.2 Communication I/O Signals Description of Connector J1 7-9
7.5.3 PCI Bus Edge Connector Pinouts 7-11
7.5.4 cPCI Bus Connector Pinouts 7-12
7.6 Power Requirements 7-12

8 Ordering Information

Appendix A MIL-STD-1553 Word Formats

Appendix B MIL-STD-1553 Message Formats

Figures

Figure 1-1 *EXC-1553PCI/MCH* Block Diagram 1-3
Figure 1-2 Direct coupled connection (one bus shown) 1-5
Figure 1-3 Transformer coupled Connection (one bus shown) 1-5
Figure 1-4 MIL-STD-1553 Bus Connection 1-6
Figure 2-1 PCI Configuration Space Header 2-2
Figure 2-2 *EXC-1553PCI/MCH* Channel Memory Map 2-10
Figure 2-3 *EXC-1553PCI/MCH* Global Registers Map 2-12
Figure 3-1 Command Block Architecture: BC Mode 3-2
Figure 3-2 Control Registers Map: BC Mode 3-3
Figure 3-3 BC Command Block Architecture 3-10
Figure 3-4 Control Word Definition 3-11
Figure 3-5 Message Control Options 3-16
Figure 3-6 Minor Frame Sequencing 3-16
Figure 3-7 Memory Architecture for BC Mode 3-17
Figure 4-1 Control Registers Map: RT Mode 4-2
Figure 4-2 Descriptor Table 4-14
Figure 4-3 RT Non-broadcast Receive Message Indexing 4-20
Figure 4-4 *EXC-1553PCI/MCH* Descriptor Block – Receive 4-20
Figure 4-5 *EXC-1553PCI/MCH* Descriptor Bock – Transmit 4-21
Figure 4-6 RT Mode #1 Descriptor Block And Circular Buffer 4-29
Figure 4-7 RT Mode #2 Descriptor Block 4-32
Figure 5-1 Control Registers Map: BM Mode 5-3
Figure 5-2 Message Information Word 5-11
Figure 5-3 Bus Monitor Block Structuring 5-13
Figure 5-4 Memory Architecture for Bus Monitor Mode 5-14
Figure 7-1 *EXC-1553PCI/MCH* Board Layout 7-2
Figure 7-2 EXC-1553cPCI/MCH Board Layout 7-3
Figure 7-3 DIP Switch SW1 with all switches set to closed /on (Select ID#0) 7-5
Figure 7-4 Connector J1 – Front View 7-8
Figure 7-5 Synchronization of a single *EXC-1553PCI/MCH* to an external system 7-10
Figure 7-6 Synchronization of an external system to a single *EXC-1553PCI/MCH* 7-10
Figure 7-7 Synchronization Between *EXC-1553PCI/MCH* Boards 7-10

Tables

Table 2-1 Base Address Registers Definition 2-6
Table 3-1 MIL-STD-1553A/B Operation: BC Mode 3-18
Table 4-1 Illegalization Register Blocks 4-11
Table 4-2 Illegalization Register Map 4-12
Table 4-3 RT Mode #2 Control Word and MIB Pointer Structure 4-31
Table 4-4 Mode Code Description 4-33
Table 4-5 MIL-STD-1553A/B Operation: RT Mode 4-37
Table 5-1 MIL-STD-1553A/B Operation: BC Mode 5-16
Table 6-1 Interrupt Ring Buffer 6-3
Table 7-1 Jumper Settings Required to Select Coupling Mode 7-6
Table 7-2 Channel Jumper Groups 7-6
Table 7-3 Connector J1 Pinouts 7-8
Table 7-4 Communication I/O Signals Descriptions of Connector J1 7-9
Table 7-5 PCI Bus Edge Connector Pinouts 7-11
Table 7-6 cPCI Bus Connector Pinouts 7-12

1 Introduction

Chapter 1 provides an overview of the *EXC-1553PCI/MCH* avionics communication board. The following topics are covered.

1.1 Overview 1-1
1.2 Installation. 1-4
1.2.1 Installing the Board 1-4
1.2.2 Adding Excalibur Software Tools 1-4
1.3 1553 Bus Connections 1-5
1.4 Note About Pointer Registers 1-7
1.5 Technical Support 1-7

This User's Manual supports both the *EXC-1553PCI/MCH* and the *EXC-1553cPCI/MCH*. Unless otherwise indicated all references to the *EXC-1553PCI/MCH* apply also to the *EXC-1553cPCI/MCH*. For mechanical and electrical differences between the PCI and the cPCI boards, see **Chapter 7 Mechanical And Electrical Specifications** on page 7-1.

1.1 Overview

The *EXC-1553PCI/MCH* is an intelligent, MIL-STD-1553 PCI interface board for avionics test and simulation applications. Available in one, two, three or four channel versions, the *EXC-1553PCI/MCH* provides a complete solution for developing and testing 1553 interfaces and performing system simulation of the MIL-STD-1553 bus. All standard variations of the MIL-STD-1553 protocol are handled by the board.

Each channel of the *EXC-1553PCI/MCH* contains 32k × 16 of dual-port RAM for Data blocks, Control registers, and Look-up tables. All Data blocks and Control registers are memory-mapped and may be accessed in real time.

Each of the independent dual-redundant 1553 channels may be programmed to operate in one of four modes of operation: Bus Controller, Remote Terminal, RT/Concurrent-Bus Monitor, and Bus Monitor. The *EXC-1553PCI/MCH* comes complete with Windows software, and a C driver software library including source code, and one mating connector.

The *EXC-1553PCI/MCH*-E option is an extended temperature (-40° to +85°C), ruggedized version of the board for industrial or harsh environmental conditions.

EXC-1553PCI/MCH and *EXC-1553cPCI/MCH* Board features

Supports up to 4 MIL-STD-1553, independent, dual-redundant channels

EXC-1553PCI/MCH Half-size PCI card
EXC-1553cPCI/MCH Standard cPCI size

Operating Environment

Humidity: 5% - 90% noncondensing
Temperature: 0° - 70°C
-40° - +85°C (Extended temp.option)

Physical Characteristics

Dimensions: PCI board. 157 mm ×107 mm
cPCI board 160 mm ×100 mm
Weight: with 4 channels 220 grams

Host Interface

PCI Compliance: Target 16 bit, 5V only
(8 and 32 bit operations may not be performed)
Memory space occupied: 512 Kbytes
Interrupts: INTA#
Power: Depends on configuration

Software Support

C Drivers with source code

Features per Channel

- Operates as BC, RT, BM or RT/Concurrent-BM
- Multiple protocol capability
  MIL-STD-1553A
  MIL-STD-1553B
- Autonomous operation in all modes
- 32K Word memory-mapped RAM
- 32 Control registers
- Polling or interrupt driven
- Real-time operation
- Built-in Test capability
- BC Mode
  Major/Minor frames
  Programmable Intermessage gap
  Automatic retry
- RT Mode
  Single RT simulation
  Subaddress double buffering
  Circular buffer mode
  Message illegalization
  16-bit Time Tag
  Programmable broadcast mode
- BM mode
  16-bit Time Tag
  Filtering per RT
  Interrupt history list
  Programmable monitor block count

See **Chapter 8: Ordering Information**, for exact part numbers.

Figure 1-1 is a block diagram of the *EXC-1553PCI/MCH*

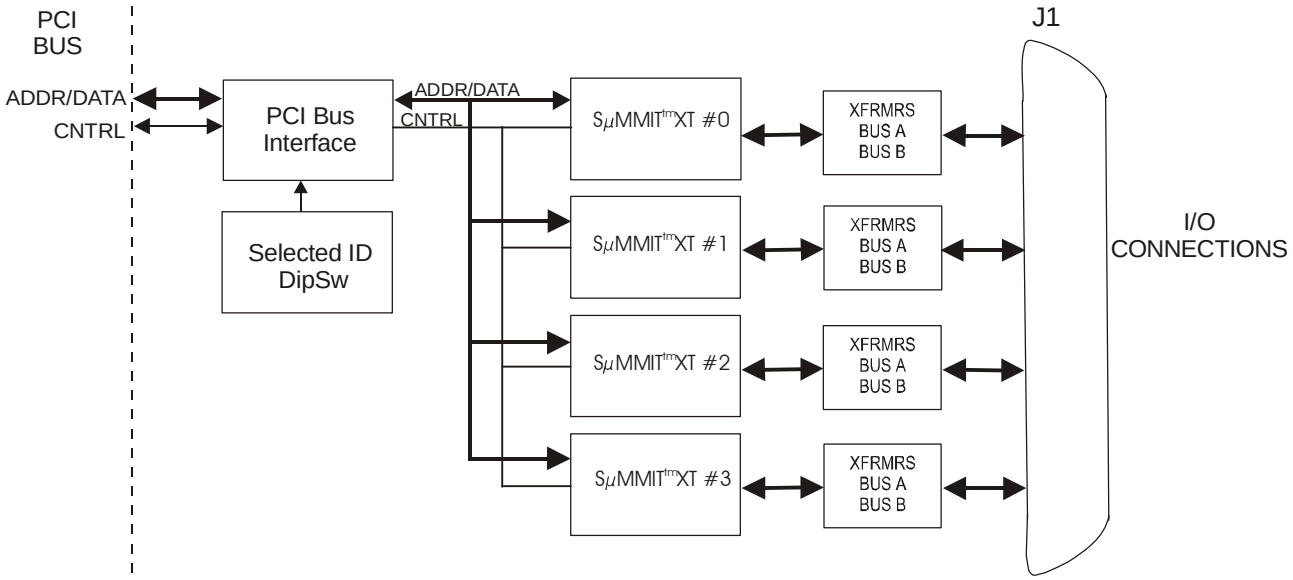


Figure 1-1 *EXC-1553PCI/MCH* Block Diagram

1.2 Installation

To operate the *EXC-1553PCI/MCH* board:

- Install the board in your computer.
- Install the *EXC-1553PCI/MCH Software Tools*.

1.2.1 Installing the Board

Installation of the *EXC-1553PCI/MCH* board is similar to that of all PCI "Local bus" boards. The *EXC-1553PCI/MCH* complies with the "Plug and Play" specification of the PCI standard. As such, its absolute address is determined by the BIOS at start-up.

Warning Wear a suitably grounded electrostatic discharge wrist strap whenever handling the Excalibur board and use all necessary antistatic precautionary measures.

To install the *EXC-1553PCI/MCH*:

1. 1553 devices may be connected to the 1553 bus either directly (direct-coupled) or via a bus-coupling stub (transformer coupled).Use JUmpers JP2–JP17 to set the coupling mode to the 1553 bus(es). See **7.4.1 Channel 0 – Channel 3 1553 Coupling Mode Select Jumpers [JP2–JP17]** on page 7-6.
2. Make certain the computer power source is disconnected. Insert the

- *EXC-1553PCI/MCH* board into any PCI compatible slot.
- EXC-1553cPCI/MCH board into any cPCI compatible slot.

3. For the *EXC-1553PCI/MCH* tighten the board's PCI bracket with the slot screw, to ground the board to the computer.
4. Attach the user-constructed cable to the board and to the communication bus. The cable may be connected to and disconnected from the board while power to the computer is turned on, but not while the board is transmitting

1.2.2 Adding Excalibur Software Tools

The standard software included with the *EXC-1553PCI/MCH* carrier board is for Windows operating systems. Software compatible with other operating systems is available and can be downloaded from our website: www.mil-1553.com

To add the Excalibur *Software Tools* drivers, see the **`readme.txt`** file on the software diskette that came with your specific board.

1.3 1553 Bus Connections

For short distances, direct coupling may be used to connect the *EXC-1553PCI/MCH* directly to another 1553 device. To ensure data integrity, you must make certain that the cable connecting the two devices is properly terminated with 78-Ohm resistors (see Figure 1-2).

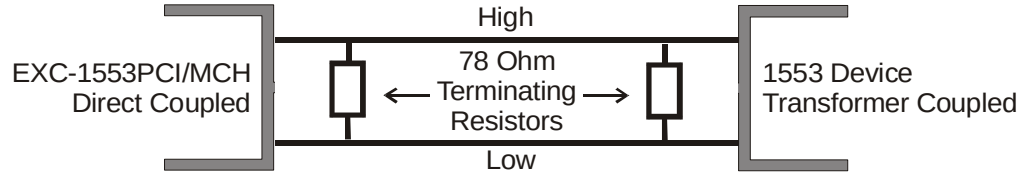


Figure 1-2 Direct coupled connection (one bus shown)

If operating in the more standard Transformer coupling mode, use stub coupler devices, which are available from Excalibur Systems. Two terminators are required for each coupler, which services a single bus, i.e. BUS A (see Figure 1-3). For more information see our website: www.mil-1553.com.

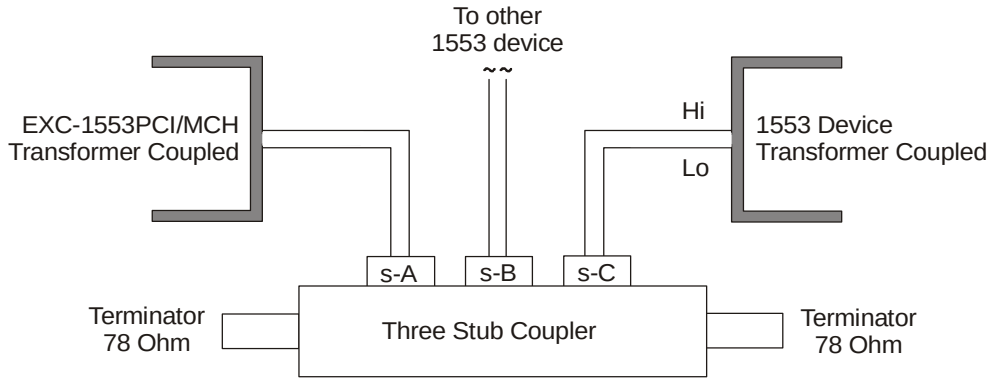


Figure 1-3 Transformer coupled Connection (one bus shown)

Example of MIL-STD-1553 Bus Connection

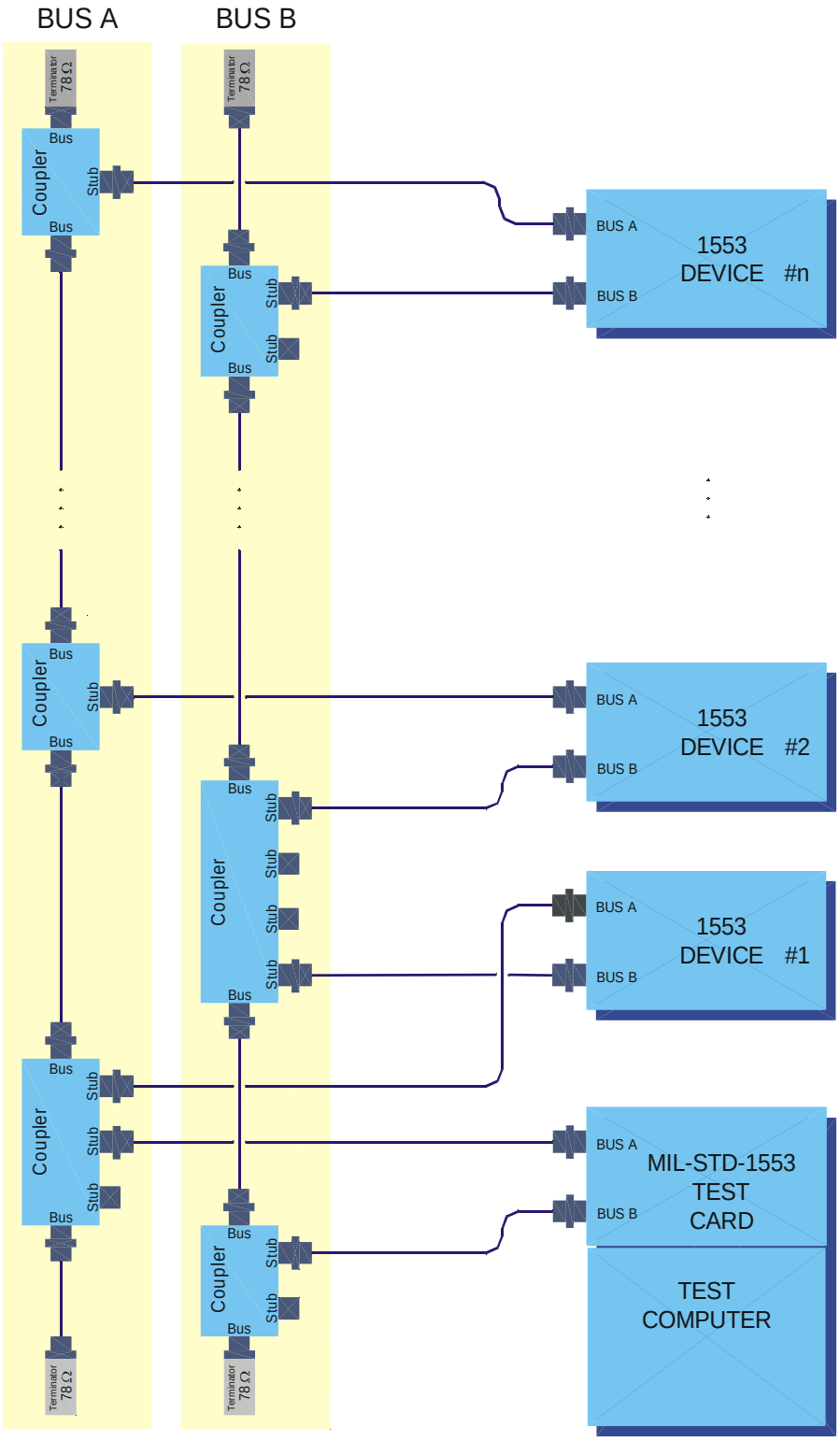


Figure 1-4 MIL-STD-1553 Bus Connection

1.4 Note About Pointer Registers

When a register's value is a pointer to an address, the value is a word address, not a byte address. However, the addresses listed in the memory maps (or control register maps) in this manual are byte addresses. To convert the word address to the byte address, multiply the address value by two.

For example, when the value of the Initial Monitor Data Pointer register (at address 0x0018) is 0x1000, the data for the first message is stored at address 0x2000, and the data for the next message will be stored in the next available memory location (after the data of the first message).

1.5 Technical Support

Excalibur Systems is ready to assist you with any technical questions you may have. For technical support, see the Technical Support section of our website: www.mil-1553.com. You can also contact us by phone. To find the location nearest you, see the Contact section of our website.

2 PCI Architecture

Chapter 2 describes the PCI architecture. The following topics are covered:

2.1 Memory Structure 2-1
2.2 PCI Configuration Space Header 2-2
2.3 PCI Configuration Registers 2-3
2.4 Channel Memory Space 2-9
2.5 Global Registers Map 2-12

2.1 Memory Structure

The *EXC-1553PCI/MCH* requests two memory blocks:

The first memory block is 512K bytes in size and contains the memory space for the channels. This block is described in detail in section **2.4 Channel Memory Space** on page 2-9.

The second memory block is 64 bytes in size and contains the Global Registers which are explained in more detail in section **2.5 Global Registers Map** on page 2-12.

2.2 PCI Configuration Space Header

The *EXC-1553PCI/MCH* includes a PCI Configuration Space Header, as required by the PCI specification. The registers contained in this header enable software to set up the Plug and Play operation of the board, and set aside system resources.

MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line	3C H
Reserved = 0s				38 H
Reserved = 0s			Cap. pointer	34 H
Expansion ROM Base Address (not used)				30 H
Subsystem ID		Subsystem Vendor ID		2C H
Cardbus CIS Pointer (not used = 0s)				28 H
Base Address Register #5 (not used)				24 H
Base Address Register #4 (not used)				20 H
Base Address Register #3 (not used)				1C H
Base Address Register #2 (not used)				18 H
Base Address Register #1 – Global Registers				14 H
Base Address Register #0 Dual-port RAM				10 H
BIST	Header Type = 0	Latency Timer	Cache Line Size	0C H
Class Code			Rev ID	08 H
Status Register		Command Register		04 H
Device ID		Vendor ID		00 H
31 24	**23 16**	**15 08**	**07 00**	

Figure 2-1 PCI Configuration Space Header

2.3 PCI Configuration Registers

2.3.1 Vendor Identification Register (VID) Address: 00–01 (H)

Power-up value 1405 H
Size: 16 bits

The Vendor Identification register contains the PCI Special Interest Group vendor identification number assigned to Excalibur Systems.

2.3.2 Device Identification Register (DID) Address: 02–03 (H)

Power-up value 4004 H
Size: 16 bits

The Device Identification register contains the *EXC-1553PCI/MCH* device identification number.

2.3.3 PCI Command Register (PCICMD) Address: 04–05 (H)

Power-up value: 0000 H
Size: 16 bits

The PCI Command register contains the PCI Command.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0s
09	**Fast Back-to Back Enable**	Always set to 0
08	**System Error Enable**	Always set to 0
07	**Address Stepping Support**	Always set to 1
06	**Parity Error Enable**	Always set to 0
05	**VGA Palette Snoop Enable**	Always set to 0
04	**Memory Write and Invalidate Enable**	Always set to 0
03	**Special Cycle Enable**	Always set to 0
02	**Bus Master Enable**	Always set to 0
01	**Memory Access Enable**	Always set to 1
00	**I/O Access Enable**	Since the *EXC-1553PCI/MCH* board does not use I/O space, the value of this register is ignored.

PCI Command Register

2.3.4 PCI Status Register (PCISTS) Address: 06–07 (H)

Power-up value: 0080 H

Size: 16 bits

The PCI Status register contains the PCI status information.

Bit	Bit Name	Description
15	**Detected Parity Error**	This bit is set whenever a parity error is detected. It functions independently from the state of Command Register Bit 6. This bit may be cleared by writing a 1 to this location.
14	**Signaled System Error**	Not used
13	**Received Master Abort**	Not used
12	**Received Target Abort**	Not used
11	**Signaled Target Abort**	This bit is set whenever this device aborts a cycle when addressed as a target. This bit can be reset by writing a 1 to this location.
09-10	**Device Select (DEVSEL#) Timing Status**	Set to 10 (slow timing)
08	**Data Parity Reported**	Not used
07	**Fast Back-to-Back Capable**	Set to 1
06	**Reserved**	
05	**66MHz capable**	Set to 0
04	**Capability List enable**	Set to 1
00-03	**Reserved**	

PCI Status Register

2.3.5 Revision Identification Register (RID) Address: 08 (H)

Power-up value: 01 H

Size: 8 bits

The Revision Identification register contains the revision identification number of the *EXC-1553PCI/MCH*.

2.3.6 Class Code Register (CLCD) Address: 09–-0B (H)

Power-up value: FF0000 H
Size: 24 bits

The Class code Register value indicates that the *EXC-1553PCI/MCH* does not fit into any of the defined class codes.

2.3.7 Cache Line Register Size Register (CALN) Address: 0C (H)

Power-up value: 00 H
Size: 8 bits

Not used

2.3.8 Latency Timer Register (LAT) Address: 0D (H)

Power-up value: 00 H
Size: 8 bits

Not used

2.3.9 Header Type Register (HDR). Address: 0E (H)

Power-up value: 00 H
Size: 8 bits

The *EXC-1553PCI/MCH* is a single function PCI device.

2.3.10 Built-In Self-Test Register (BIST) Address: 0F (H)

Power-up value: 00 H
Size: 8 bits

The Built-In Self-Test register is not implemented in the *EXC-1553PCI/MCH*.

2.3.11 Base Address Registers (BADR)

Address: 10, 14, 18, 1C, 20, 24 (H)

Power-up value: 00000000 H for each

Size: 32 bits

The Base Address Registers are used by the system BIOS to determine the number, size and base addresses of memory pages required by the board, within host address space.

Two memory pages are required by the *EXC-1553PCI/MCH:* one for the dual-port RAM and one for the Global Registers.

Register	Offset	Size	Function
Base Address 0	10 H	512 K Byte	Dual-port RAM
Base Address 1	14 H	64 Byte	Global registers

Table 2-1 Base Address Registers Definition

Each Base Address Register contains 32 bits:

Bit	Description
04-31	Address of memory region (with lower 4 bits removed)
03	Always 0 – memory is not prefetchable
01-02	Always 0 – memory may be mapped anywhere
00	Always 0 – indicates memory space

Base Address Register

2.3.12 Cardbus CIS Pointer

Address: 28 (H)

Power-up value: 00000000 H

Size: 32 bits

The Cardbus Pointer is not implemented on the *EXC-1553PCI/MCH*.

2.3.13 Subsystem ID

Address: 2C (H)

Power-up value: 0000 H
Size: 16 bits

2.3.14 Subvendor ID

Address: 2E (H)

Power-up value: 0000 H
Size: 16 bits

2.3.15 Expansion ROM Base Address Register (XROM)

Address: 30 (H)

Power-up value: 00000000 H
Size: 32 bits

The Expansion ROM Space is not implemented on the *EXC-1553PCI/MCH*.

2.3.16 Reserved

Address: 34–3A (H)

Power-up value: 0000000000000000 H
Size: 64 bits

2.3.17 Interrupt Line Register (INTLN)

Address: 3C (H)

Power-up value: 00 H
Size: 8 bits

The Interrupt Line register indicates the interrupt routing for the PCI Controller. The value of this register is system-architecture specific. For *x*86-based PCs, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines; the values of 1 to F (H) correspond with the IRQ numbers 1 through 15, and the values from 10(H) to FE (H) are reserved. The value of 255 signifies either “unknown” or “no connection” for the system interrupt.

2.3.18 Interrupt Pin Register (INTPIN) Address: 3D (H)

Power-up value: 01 H
Size: 8 bits

Set to INTA#

2.3.19 Minimum Grant Register (MINGNT) Address: 3E (H)

Power-up value: 00 H
Size: 8 bits

The Minimum Grant register is not implemented on the *EXC-1553PCI/MCH*.

2.3.20 Maximum Latency Register (MAXLAT) Address: 3F (H)

Power-up value: 00 H
Size: 8 bits

The Maximum Latency register is not implemented on the *EXC-1553PCI/MCH*.

2.4 Channel Memory Space

The Channel Memory Space resides in the first memory block.

The 523 Kbytes of memory is broken up into four memory blocks of 128 Kbyte. Each 128 Kbyte memory block represents the Address Space of a specific channel. Each Channel Address Space is shared between the:

- Channel Register Block, for the 32 control registers
- Channel Memory Block, for 1553 Message / Control Data storage
- Channel External Timer Clock Register, to set the external timer clock value and the
- Channel Reset Register to carry out the software reset of the channel.

For each channel a powerful RISC processing unit (UTMC "SμMMIT™-XT" 1553 protocol controller) provides automatic message handling, message status, general operational status and interrupt information. The user has direct access to all control registers and data blocks in Real Time. The *EXC-1553PCI/MCH* may be configured to support MIL-STD-1553A as well as MIL-STD-1553B protocol.

Channel 3	Reserved	70000 – 7FFFF H
	Channel Reset Register	6FFFE H
	Channel External Time Clock Register	6FFFC H
	Channel Memory Block (1553 Message/Control Data Storage)	60040 – 6FFFB H
	Channel Registers Block (32 Control Registers)	60000 – 6003F H
Channel 2	Reserved	50000 – 5FFFF H
	Channel Reset Register	64FFFE H
	Channel External Time Clock Register	4FFFC H
	Channel Memory Block (1553 Message/Control Data Storage)	60040 – 6FFFB H
	Channel Registers Block (32 Control Registers)	40000 – 4003F H
Channel 1	Reserved	30000 – 3FFFF H
	Channel Reset Register	2FFFE H
	Channel External Time Clock Register	2FFFC H
	Channel Memory Block (1553 Message/Control Data Storage)	20040 – 2FFFB H
	Channel Registers Block (32 Control Registers)	20000 – 2003F H
Channel 0	Reserved	10000 – 1FFFF H
	Channel Reset Register	0FFFE H
	Channel External Time Clock Register	0FFFC H
	Channel Memory Block (1553 Message/Control Data Storage)	00040 – 0FFFB H
	Channel Registers Block (32 Control Registers)	00000 – 0003F H

Figure 2-2 *EXC-1553PCI/MCH* Channel Memory Map

Chapters 3, 4 and 5 of the *User's Manual* explain the operation of the channels of the *EXC-1553PCI/MCH* in each of the three modes: Bus Controller, Remote Terminal, and Bus Monitor. In each chapter the mode specific Control Registers and Memory Block are described.

2.4.1 Channel External Timer Clock Register

Address: 0FFFC, 2FFFC, 4FFFC, 6FFFC (H) Read/Write

The Channel External Timer Clock Register selects the external timer clock value for the channel's timer. In normal operation, the channel uses an internal fixed clock (64 μsec.). However, the channel can be programmed to use an external, user-defined clock. (See the ETCE (bit 10) in Bus Controller **Control Register** on page 3-4 and Bus Monitor Mode **Control Register** on page 5-4.)

A hardware or software reset will reset the external timer clock to its default value (64 μsec). The external timer clock has a range of 4 μsec (250 KHz) to 126 μsec (8 KHz)

Bit	Description
06-15	Don't care
00-05	Timer Clock Value **Valid values:** 0001(H) (250 KHz) – 003E (H) (7.94 KHz)

Channel External Timer Clock Register

To formulate the Timer Clock Value (TCV):

$$TCV = \frac{1,000,000}{2 \times F} - 1$$

F = Desired frequency (HZ) — 7.94 KHz–250 KHz

Example: Desired programmable Timer Clock frequency is 10 KHz (100 μsec) resolution:

$$TCV = \frac{1,000,000}{2 \times 10,000} - 1 = (50 - 1) = 49\text{Dec} = 31(\text{H})$$

Write 00031 H to the register.

2.4.2 Channel Reset Register

Address: 0FFFE, 2FFFE, 4FFFE, 6FFFE (H) Read/Write

Writing to a Channel Reset Register (data = don't care), performs a software reset of that channel. The channel will act as if the power had been switched off and then on; encoder, decoder, all control registers and associated logic will be reset

Note Writing to this register immediately terminates command processing. The reset operation takes 5 μsec to execute.

2.5 Global Registers Map

The board global registers reside in the second memory block.

Board ID	00 H
Software Reset	02 H
Interrupt Status	04 H
Interrupt Reset	06 H
Channel 0 Info	08 H
Channel 1 Info	0A H
Channel 2 Info	0C H
Channel 3 Info	0E H
External Timer Clock Source Register	10 H
Reserved	12 – 3F H

Figure 2-3 *EXC-1553PCI/MCH* Global Registers Map

2.5.1 Board Identification Register

Address: 0 (H)
Length 16bits

The Board Identification register comprises three identification items.

Bit	Description
08-15	Hard coded to the value 40 H
04-07	FPGA revision
00-03	Selected ID

Board Identification Register

2.5.2 Software Reset Register

Address: 2 (H)
Length 16bits

The Software Reset register performs reset operations of the channels. Individual channels may be reset.

Bit	Description	
04-15	Reserved – set to 0	
03	Channel 3 reset	1 = reset channel 0 = no effect
02	Channel 2 reset	1 = reset channel 0 = no effect
01	Channel 1 reset	1 = reset channel 0 = no effect
00	Channel 0 reset	1 = reset channel 0 = no effect

Software Reset Register

2.5.3 Interrupt Status Register

Address: 4 (H)
Length 16 bits

The Interrupt Status register indicates which channels are currently interrupting.

Bit	Description
04-15	Reserved – set to 0
03	1 = indicates that channel 3 is interrupting
02	1 = indicates that channel 2 is interrupting
01	1 = indicates that channel 1 is interrupting
00	1 = indicates that channel 0 is interrupting

Interrupt Status Register

2.5.4 Interrupt Reset Register

Address: 6 (H)
Length 16 bits

The Interrupt Reset register resets the interrupting channels by writing to the relevant bits of the register.

Bit	Description
04-15	Reserved – set to 0
03	1 = resets channel 3 interrupt 0 = no effect
02	1 = resets channel 2 interrupt 0 = no effect

Interrupt Reset Register

Bit	Description
01	1 = resets channel 1 interrupt 0 = no effect
00	1 = resets channel 0 interrupt 0 = no effect

Interrupt Reset Register

2.5.5 Channel Info Registers

Address: 08, 0A, 0C, 0E (H)
Length 16 bits each

The Channel Info Registers provide identification information for each of the four channels, respectively.

Bit	Description	
12-15	Channel ID	00 H = Channel 0 Info register 01 H = Channel 1 Info register 02 H = Channel 2 Info register 03 H = Channel 3 Info register
05-11	Reserved – set to 0	
00-04	Channel detect	03 H = Channel present 1F H = No channel installed

Channel Info Registers

2.5.6 External Timer Clock Source Register

Address: 10 (H)
Length 16 bits

The External timer Clock Source Register is used by all the channels to set either an internal or external source for the External Timer Clock. See section **2.4.1**. **Channel External Timer Clock Register** on page 2-11.

Bit	Description	
01-15	Reserved – set to 0	
00	External Timer Clock Source	1 = External Source 0 = Internal Source (**Default**)

Time Tag Clock Select Register

If an external source is used, take care to ensure that it is as close to 1 MHz as possible, otherwise deviations the desired external clock will occur. See section **7.5.2 Communication I/O Signals Description of Connector J1** on page 7-9.

3 Bus Controller Operation

Chapter 3 describes *EXC-1553PCI/MCH* operation in Bus Controller (BC) mode. The topics covered are:

3.1 Bus Controller Message Processing 3-2
3.2 Control Registers: BC Mode 3-3
3.3 BC Architecture 3-10
3.3.1 Control Word 3-11
3.3.2 1553 Command Words 3-14
3.3.3 Data Pointer 3-15
3.3.4 1553 Status Words 3-15
3.3.5 Branch Address 3-15
3.3.6 Timer Value 3-15
3.4 Command Block Chaining 3-16
3.5 Memory Architecture 3-17
3.6 MIL-STD-1553A/B Operation: BC Mode 3-18

3.1 Bus Controller Message Processing

To process messages, the *EXC-1553PCI/MCH* uses data supplied in the control registers along with data stored in RAM memory. The channel accesses eight words stored in RAM memory called a command block. The command block is accessed at the beginning and end of command processing.

Note In BC mode, the channel does not need to re-read the Command Block on a retry situation.

The user allocates memory spaces for the minor frame. The top of the command blocks can reside at any address location. Defined and entered into memory by the user, the control registers are linked to the Command Block via the Command Block Pointer Register contents. Each command block contains a:

Control Word
Command Word1
Command Word2
Data Pointer
Status Word 1
Status Word 2
Branch Address
Timer Value

Figure 3-1 Command Block Architecture: BC Mode

See section **3.3 BC Architecture**, on page 3-10, for a description of each location.

Control Word information allows the channel to control the commands transmitted over the 1553 bus. The Control word allows the channel to transmit commands on a specific bus, perform retries, initiate RT-to-RT transfers, and interrupt on certain conditions. The host defines each Command Word associated with each command block. For normal 1553 commands, only the first Command Word location will contain valid data. For RT-to-RT commands, as specified in the Control Word, the host must define the first Command Word as a receive and the second Command Word as a transmit.

For a receive command, the Data Pointer is read to determine where Data Words are retrieved. The channel retrieves Data Words sequentially from the address specified by the Data Pointer. For a transmit command, the Data Pointer is read to determine the top memory location. The channel stores Data Words sequentially from this top memory location.

The channel reads the command block during minor frame processing. The channel then begins the acquisition of Data Words for either transmission or storage.

After transmission or reception, the channel begins post-processing. The command block is updated. The channel modifies the Control Word as required. An optional interrupt log entry is performed after the command block update.

3.2 Control Registers: BC Mode

The control registers are read/write unless otherwise stated. All control registers must be accessed in word mode. All control register bits are active high and are reset to 0 unless otherwise stated.

Figure 3-2 below illustrates the control registers for Bus Controller mode.

Reserved	0012 - 003E H
Command Block Pointer Register	0010 H
Minor Frame Timer	000E H
BIT Word Register	000C H
Interrupt Log List Pointer Register	000A H
Pending Interrupt Register	0008 H
Interrupt Mask Register	0006 H
Current Command Block Register	0004 H
Operational Status Register	0002 H
Control Register	0000 H

Figure 3-2 Control Registers Map: BC Mode

3.2.1 Control Register

Address: 0000 (H)
Read/Write

Use the Control register to configure the channel for BC mode operation. To make changes to the BC and this register, the STEX bit (Bit 15) must be logic 0

Bit	Bit Name	Description
15	**STEX**	Start Execution 1 = Initiates channel operation 0 = Inhibits channel operation After execution begins, writing a logic 0 will halt the channel after completing the current 1553 message.
14	**SBIT**	Start BIT 1 = Places the channel into the Built-In Test routine. The BIT test takes 1 msec. to execute and has a fault coverage of 93.4%. Once the channel has been started, the host must halt the channel in order to place it into the Built-In Test mode (STEX = 0). **Note** If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
11-13	**Reserved**	Set to 0
10	**ETCE**	External Timer Clock Enable 1 = Enables an external clock used with an internal counter for variable minor frame timing **Note** The user can only change the clock frequency before starting the device (i.e. setting bit 15 of register 0 to a login 1.
09	**ERTO**	Extended Response Time-Out 1 = Enables the extended response time-out option and forces the BC Mode to look for an RTs response time in 30 μsec. or generate time-out errors. 0 = Enables for the standard time-out in 14 μsec.
05-08	**Reserved**	Set to 0
04	**BCEN**	Broadcast Enable 1 = Enables the broadcast option for BC Mode. 0 = Enables Remote Terminal #31 as a unique remote terminal address. When enabled, the channel does not expect a Status Word response from the Remote Terminal.
03	**Reserved**	Set to 0
02	**PPEN**	Ping-Pong Enable. This bit controls the method by which the channel will retry messages. 1 = Allows the channel to ping-pong between buses during retries. 0 = All retries will be performed on the programmed bus as defined in the Retry Number field of the Command Block control word.
01	**INTEN**	Interrupt Log List Enable. 1 = Enables the interrupt log list. 0 = Prevents the logging of interrupts as they occur.
00	**Reserved**	Set to 0

Control Register

3.2.2 Operational Status Register

Address: 0002 (H)
Read/Write

The Operational Status Register provides pertinent status information for BC Mode and is not reset to 0000H on reset. Instead, the bit A/B_STD is set to 1.

Note To make changes to the BC and this register, the STEX bit (Bit 15 in the Control Register) must be logic 0.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**MSEL1**	Mode Select 1. In conjunction with Mode Select 0, this bit determines the channel's mode of operation.
08	**MSEL0**	Mode Select 0. In conjunction with Mode Select 1, this bit determines the channel's mode of operation.

MSEL1	MSEL0	Mode of Operation
0	0	BC
0	1	RT
1	0	BM
1	1	RT/ Concurrent BM Mode

07	**A/B_STD**	Military Standard 1553A or 1553B. This bit determines if the channel will operate under MIL-STD-1553A or 1553B protocol. 1 = Forces the channel to look for all responses in 9 μsec. or generate time-out errors. 0 = Automatically allows the channel to operate under the MIL-STD-1553B protocol (see section **3.6 MIL-STD-1553A/B Operation: BC Mode**, on page 3-18,
04-06	**Reserved**	These read-only bits are not applicable.
03	**EX**	Channel Executing. This read-only bit indicates whether the channel is presently executing or is idle. 1 = The channel is executing. 0 = The channel is idle.
02	**Reserved**	This read-only bit is not applicable.
01	**Ready**	Channel-Ready. This read-only bit is cleared on reset. 1 = The channel has completed initialization or BIT, and regular operation may begin.
00	**TERACT**	Channel Terminal Active. This read-only bit is cleared on reset. 1 = The channel is presently processing a 1553 message. **Note** When STEX transitions from 1 to 0, EX and TERACT stay active until command processing is complete.

Operational Status Register

3.2.3 Current Command Register

Address: 0004 (H
Read only

The Current Command register contains the last 1553 command that was transmitted by the channel. Upon the execution of each Command Block, this register will automatically be updated. This register is updated when transmission of the Command Word begins. In an RT-to-RT transfer, the register will reflect the latest Command Word as it is transmitted.

Bit	Bit Name	Description
00-15	**CC[15-0]**	Current Command. These bits contain the latest 1553 command that was transmitted by the Bus Controller.

Current Command Register

3.2.4 Interrupt Mask Register

Address: 0006 (H)
Read/Write

The BC Mode interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked only if the corresponding bit of this register is set to a logic 0.

Bit	Bit Name	Description
12-15	**Reserved**	Set to 0
11	**MERR**	Message Error Interrupt
06-10	**Reserved**	Set to 0
05	**EOL**	End Of List Interrupt
04	**ILLCMD**	Illegal Command Interrupt
03	**ILLOP**	Illogical Opcode Interrupt
02	**RTF**	Retry Fail Interrupt
01	**CBA**	Command Block Accessed Interrupt
00	**Reserved**	Set to 0

Interrupt Mask Register

3.2.5 Pending Interrupt Register

Address: 0008 (H)
Read only

The Pending Interrupt register is used to identify which of the interrupts occurred during operation. The assertion of any bit in this register generates an interrupt.

Note All register bits are cleared on a host read.

Bit	Bit Name	Description
12-15	**Reserved**	Ignore on read.
11	**MERR**	Message Error Interrupt 1 = A message error occurred. The channel can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated (if not masked) after message processing is complete.
06-10	**Reserved**	Ignore on read.
05	**EOL**	End Of List Interrupt. 1 = The channel is at the end of the command block.
04	**ILLCMD**	Illogical Command Interrupt. The channel checks for RT-to-RT Terminal address field match, RT-to-RT transmit/ receive bit mismatch and correct order, and broadcast transmit commands. If illogical commands occur, the channel will halt execution. 1 = An illogical command (i.e., Transmit Broadcast or improperly formatted RT-to-RT message) has been written into the Command Block.
03	**ILLOP**	Illogical Opcode Interrupt. 1 = An illogical opcode (i.e., any reserved opcode) was used in the command block. The channel halts operation if this condition occurs.
02	**RTF**	Retry Fail Interrupt. 1 = All programmed retries failed.
01	**CBA**	Command Block Accessed Interrupt. 1 = A command block was accessed (Opcode 1010), if enabled.
00	**Reserved**	Ignore on read.

Pending Interrupt Register

3.2.6 Interrupt Log List Pointer Register

Address: 000A (H)
Read/Write

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts.

The *EXC-1553PCI/MCH* architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K-word memory space. Initialize the lower 5 bits of this register to a logic 0 by the host. The channel controls the lower 5 bits to implement the ring-buffer architecture. Read this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Bit	Bit Name	Description
00-15	**ILLP[15-0]**	Interrupt Log List Pointer Bits. **Note** Bits 05-15 indicate the starting Base address while bits 00-04 indicate the ring location of the Interrupt Log List.

Interrupt Log List Pointer Register

3.2.7 BIT Word Register

Address: 000C (H)
Read/Write

The BIT Word register contains information on the current status of the channel hardware. The user defines the lower 8 bits of this register.

Bit	Bit Name	Description
15	**DMAF**	DMA Fail. 1 = All the channel's internal DMA activity was not completed within 16 μsec.
14	**WRAPF**	Wrap Fail. The channel automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is set. The loopback path is via the MIL-STD-1553 bus transceiver.
13	**Reserved**	Ignore on read
12	**BITF**	BIT Fail. 1 = A BIT failure. Interrogate bits 11 through 08 to determine the specific failure.
11	**BUAF**	Bus A Fail. 1 = A BIT test failure in Bus A.
10	**BUBF**	Bus B Fail. 1 = A BIT test failure in Bus B.
09	**MSBF**	Memory Test Fail. Most significant memory byte failure.
08	**LSBF**	Memory Test Fail. Least significant memory byte failure.
00-07	**UDB[7-0]**	User-Defined Bits.

BIT Word Register

3.2.8 Minor Frame Time Register

Address: 000E (H)
Read only

The Minor Frame Timer register (MFT) reflects the state of the 16-bit MFT counter. This counter is loaded via the Load Minor Frame Timer opcode (Opcode 1110).

Bit	Bit Name	Description
00-15	MFT[15-0]	Minor Frame Timer. These bits indicate the value of the timer.

Minor Frame Time Register

3.2.9 Command Block Pointer Register

Address: 0010 (H)
Read/Write

The Command Block Pointer register contains the location to start the Command Blocks. After execution begins, this register is automatically updated with the address of the next block.

Bit	Bit Name	Description
00-15	CBA[15-0]	Command Block Address. These bits indicate the starting location of the Command Block.

Command Block Pointer Register

3.3 BC Architecture

As defined in MIL-STD-1553, the Bus Controller initiates all communications on the bus. To comply with MIL-STD-1553 bus controller requirements, the *EXC-1553PCI/MCH* uses a Command Block architecture that takes advantage of both control registers and RAM. Each Command Word transmitted over the bus must be associated with a Command Block. The Command Block requires eight contiguous 16-bit memory locations for each message.

These eight locations include a:

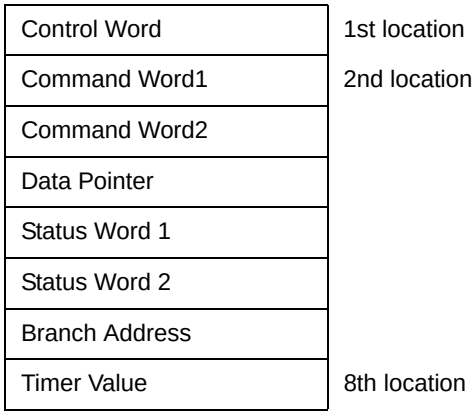


Figure 3-3 BC Command Block Architecture

The host must initialize each of the locations associated with each Command Block. The exception is for the two status locations that will be updated as Command Words are transmitted and corresponding Status Words are received. Command Blocks may be linked together in such a manner as to allow the generation of Major and Minor message frames. In addition, the BC can detect the assertion of Status Word bits and generate interrupts or branch to a new message frame, depending of course, on the specific conditions that arise.

3.3.1 Control Word

The first memory location of each BC Mode Command Block contains the Control word. Each control word contains the opcode, retry number, bus definition, RT-to-RT instruction, condition codes, and the block access message error. The control word is defined below:

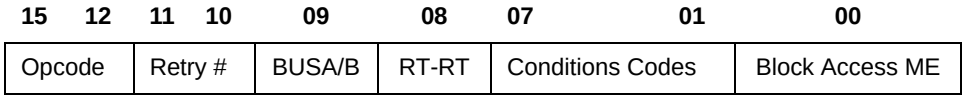


Figure 3-4 Control Word Definition

Bit	Bit Name	Description
12-15	**Opcode**	These bits define the opcode to be used by the channel for that particular Command Block. If the opcode does not perform any 1553 function, all other bits are ignored. Each of the available opcodes is defined in section **3.3.1.1 OPCODE DEFINTION**, on page 3-12,
10-11	**Retry Number**	These bits define the number of retries for each individual Command Block and if retry opcode is used. If the Ping-Pong Enable Bit (bit 02 of the Control Register) is not enabled, all retries will occur on the programmed bus. However, if bit 02 is enabled, the first retry will always occur on the alternate bus, the second retry will occur on the primary bus, the third retry will occur on the alternate bus, and the fourth retry will occur on the primary bus. **Bit 11 / Bit 10 / No. of Retries** 0 / 1 / 1 1 / 0 / 2 1 / 1 / 3 0 / 0 / 4
09	**Bus A/B**	This bit defines on which of the two buses the command will be transmitted (i.e., primary bus). (Logic 1 = Bus A, Logic 0 = Bus B).
08	**RT-RT Transfer**	This bit defines whether or not the present Command Block is an RT-to-RT transfer and if the channel should transmit the second command word. Data associated with an RT-to-RT is always stored by the channel.
01-07	**Condition Codes**	These bits define the condition code the channel uses for that particular Command Block. Each of the available condition codes is defined in section**3.3.1.2 BC CONDTION CODES**, on page 3-14,
00	**Block Access Message Error**	The channel sets this bit to 1, indicating a protocol message error occurred in the RT's response. For this occurrence, the channel will overwrite this bit prior to storing the Control Word into memory. An example of this type of error would be noise on the 1553 bus.

Control Word Description

3.3.1.1 OPCODE DEFINTION

Opcode	Field Name	Definition
0000	**End Of List**	This opcode instructs the channel that the end of the command block has been encountered. Command processing stops and the interrupt is generated if the interrupt is enabled. No command processing takes place (i.e., no 1553).
0001	**Skip**	This opcode instructs the channel to load the message-to-message timer with the value stored in timer value location. The channel will then wait the specific time before proceeding to the next command block. This opcode allows for scheduling a specific time between message execution. No command processing takes place (i.e., no 1553).
0010	**Go To**	This opcode instructs the channel to “go to” the command block as specified in the branch address location. No command process takes place (i.e., no 1553).
0011	**Built-in Test**	This opcode instructs the channel to perform an internal built-in test. If the channel passes the built-in test, then processing of the next command block will continue. However, if the channel fails the built-in test, then processing stops. No command processing takes place (i.e., no 1553).
0100	**Execute Block; Continue**	This opcode instructs the channel to execute the current command block and proceed to the next command block. This opcode allows for continuous operations.
0101	**Execute Block; Branch**	This opcode instructs the channel to execute the current command block and unconditionally branch to the location as specified in the branch address location.
0110	**Execute Block; Branch on Condition**	This opcode instructs the channel to execute the current command block and branch only if the condition is met. If no conditions are met, the opcode appears as an execute and continue.
0111	**Retry on Condition**	This opcode instructs the channel to perform automatic retries, as specified in the control word, if particular conditions occur. If no conditions are met, the opcode appears as an execute and continue.
1000	**Retry on Condition; Branch**	This opcode instructs the channel to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met, the channel retries. Once all retries have executed, the channel branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and branch.
1001	**Retry on Condition; Branch if all Retries Fail**	This opcode instructs the channel to perform automatic retries, as specified in the control word, if particular conditions occur. If the conditions are met and all the retries fail, the channel branches to the location as specified in the branch address location. If no conditions are met, the opcode appears as an execute and continue.

Opcode Definition

Opcode	Field Name	Definition
1010	**Interrupt; Continue**	This opcode instructs the channel to interrupt and continue processing on the next command block. When using this opcode, no 1553 processing occurs.
1011	**Call**	This opcode instructs the channel to “go to” the command block as specified in the branch address location without processing this block. The next command block address is saved in an internal register so that the channel may remember one address and return to the next command block. No command processing takes place (i.e., no 1553).
1011	**Call**	This opcode instructs the channel to “go to” the command block as specified in the branch address location without processing this block. The next command block address is saved in an internal register so that the channel may remember one address and return to the next command block. No command processing takes place (i.e., no 1553).
1100	**Return to Call**	This opcode instructs the channel to return to the command block address saved during the Call opcode. No command processing takes place (i.e., no 1553).
1101	**Reserved**	The channel will generate an illegal opcode interrupt (if interrupt enabled) and automatically stop execution if a reserved opcode is used.
1110	**Load Minor Frame Timer**	This opcode instructs the channel to load the minor frame timer (MFT) with the value stored in the eighth location of the current command block. The timer will be loaded after the previous MFT has decremented to zero. After the MFT timer is loaded with the new value, the channel will proceed to the next command block. No command processing takes place (i.e., no 1553).
1111	**Return to Branch**	This opcode instructs the channel to return to the command block address saved during a Branch opcode. No command processing takes place (i.e., no 1553).

Opcode Definition (Continued)

Note For entries with interrupts enabled, all interrupts are logged after message processing is completes.

3.3.1.2 BC CONDTION CODES

Condition codes have been provided as a means for the *EXC-1553PCI/MCH* to perform certain functions based on the RT's Status Word. In an RT-to-RT transfer, the conditions apply to both of the Status Words. Each bit of the condition codes is defined below.

Bit Number	Description
07	Message Error. This condition will be met if the channel detects an error in the RT's response, or if it detects no response. The channel will wait 15 μsec. in 1553B mode and 9 μsec. in 1553A mode before declaring an RT no response (see section **3.6 MIL-STD-1553A/B Operation: BC Mode**, on page 3-18,).
06	Status Word Response with the Message Error bit set (Bit time 09 in 1553A mode). This condition is met if the channel detects that the RT's Status Word has the Message Error bit set.
05	Status Word Response with the Busy bit set (Bit time 16 in 1553A mode). This condition is met if the channel detects that the RT's Status Word has the Busy bit set.
04	Status Word Response with the Terminal Flag bit set (Bit time 19 in 1553A mode). This condition is met if the channel detects that the RT's Status Word has the Terminal Flag bit set.
03	Status Word Response with the Subsystem Fail bit set (Bit time 17 in 1553A mode). This condition is met if the channel detects that the RT's Status Word has the Subsystem Fail bit set.
02	Status Word Response with the Instrumentation bit set (Bit time 10 in 1553A mode). This condition is met if the channel detects that the RT's Status Word has the Instrumentation bit set.
01	Status Word Response with the Service Request bit set (Bit time 11 in 1553A mode). This condition is met if the channel detects that the RT's Status Word has the Service Request bit set.

Condition Codes

3.3.2 1553 Command Words

The next two locations of the BC Mode Command Block are for 1553 Command Words. In most 1553 messages, only the first Command Word needs to be initialized. However, in an RT-to-RT transfer, the first Command Word is the Receive Command and the second Command Word is the Transmit Command.

3.3.3 Data Pointer

The fourth location of the BC Mode Command Block is the data pointer that points to the first memory location to store or retrieve the Data Words associated with the message for that command block. This data structure allows the channel to store or retrieve the exact specified number of Data Words, thus saving memory space and providing efficient space allocation.

Note In an RT-to-RT transfer, the channel uses the data pointer as the location in memory to store the transmitted data in the transfer.

One common application for the data pointer occurs when the channel needs to send the same data words to several RTs. Here, each Command Block associated with those messages would contain the same data pointer value, and, therefore, retrieve and transmit the same data. Note that the Data Pointer is never updated (i.e., the channel reads and writes the pointer but never changes its value).

3.3.4 1553 Status Words

The next two locations in the BC Mode Command Block are for Status Words. As the RT responds to the BC's command, the corresponding Status Word will be stored in Status Word 1. In an RT-to-RT transfer, the first Status Word will be the status of the Transmitting RT while the second Status Word will be the status of the Receiving RT.

3.3.5 Branch Address

The seventh location in the BC Mode Command Block contains the starting location of the branch. This location simply allows the channel to branch to another location in memory when certain opcodes are used.

3.3.6 Timer Value

The last location in the BC Mode Command Block is the Timer Value. This timer is used:

- To set up minor frame schedules when using the Load Minor Frame Timer opcode (1110). The MFT counter is clocked by a 15.625 KHz. (64 μsec.) internal clock. The MFT counter runs continuously during message processing and must decrement to zero prior to loading the next Minor Frame time value.
- As a message-to-message timer (MMT) when using the Skip opcode (0001). The MMT timer is clocked at the 24 MHz (41.666 nsec.) rate and allows for scheduling of specific time between message execution.

3.4 Command Block Chaining

To determine the first Command Block, set the initial start address in the Command Block Pointer Register [Address 0010 (H)]. The Command Blocks will execute in a contiguous fashion as long as no “go to”, “branch”, “call”, or “return” opcodes are used. With the use of these opcodes, almost any memory configuration is possible. Figures 3-5 and 3-6 show how several Command Blocks may be linked together to form a command frame and how branch opcodes may be used to link minor frames. The minimum BC intermessage gap is 28.0 μsec.

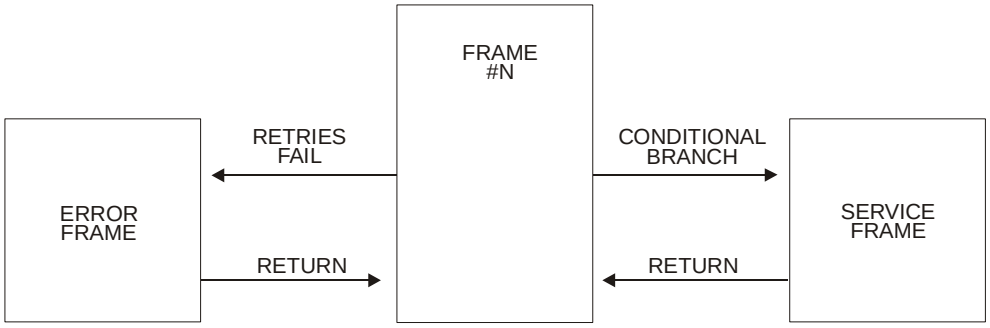


Figure 3-5 Message Control Options

The example in Figure 3-6 shows a configuration of four minor frames, in which Message A is sent in every frame, Message B is sent in every other frame, and Message C is sent once. Each minor frame goes out at 10 msec. (100Hz). If each minor frame is 10 μsec. long, Message A is sent every 10 msec., Message B is sent every 20 μsec., and Message C is sent every 40 μsec.

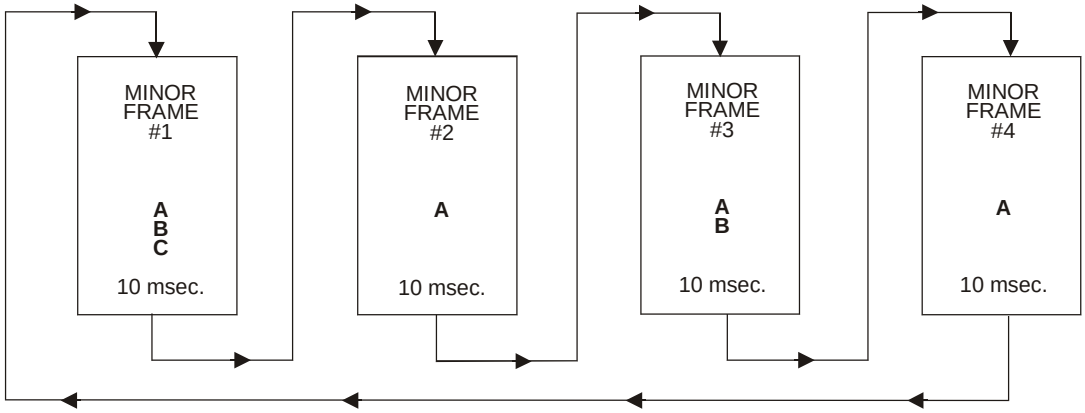


Figure 3-6 Minor Frame Sequencing

3.5 Memory Architecture

After reviewing the control registers, it is advantageous to look at how to set up memory to configure the *EXC-1553PCI/MCH* as a Bus Controller. This section shows one method for defining the memory configuration.

The configuration shows the Command Blocks, data locations, and the Interrupt Log List as separate entities. Figure 3-7 shows that the first block of memory is allocated for the Command Blocks. Notice that the Command Block Pointer Register initially points to the control word of the first Command Block. After completing execution of that first Command Block, the Command Block Pointer Register will automatically be updated to show the address of the next Command Block.

Following the Command Block locations is the memory required for all the data words. In BC applications, the number of data words for each Command Block is known. In Figure 3-7, for example, the first Command Block has allocated several memory locations for expected data. Conversely, the second Command Block has only allocated a few memory locations. Since the number of data words associated with each Command Block is known, memory may be used efficiently.

Also shown as a separate memory area is the Interrupt Log List (see **Interrupt Log List Pointer Register**, on page 3-8,). Notice that the Interrupt Log List Pointer Register points to the top of the initial Log List. After execution of that first BC Command Block, the Interrupt Log List Pointer Register will automatically be updated if interrupt condition exists.

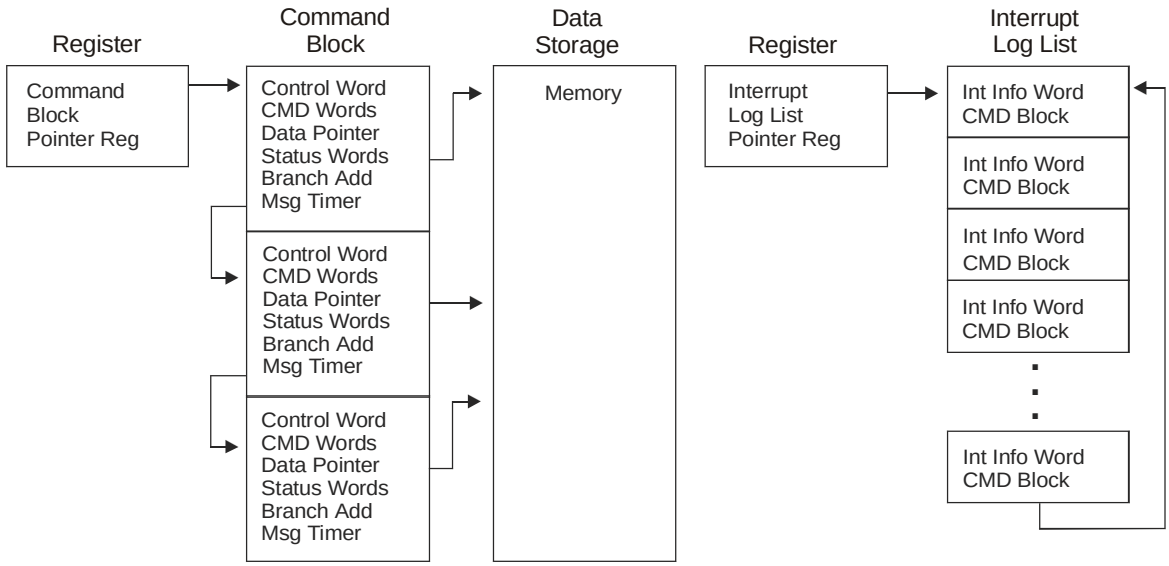


Figure 3-7 Memory Architecture for BC Mode

3.6 MIL-STD-1553A/B Operation: BC Mode

To maximize flexibility, the *EXC-1553PCI/MCH* can operate in many different systems that use various protocols. Specifically, two of the protocols that the channel may be used with are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, configure the channel through the Control register (ERTO Bit 09) and the Operational Status register (A/B_STD Bit 07). Table 3-1 defines the four ways to program the *EXC-1553PCI/MCH*.

A/B_STD	ERTO	RESULT
0	0	1553B standard, 1553B response (in 14 μsec.)
0	1	1553B standard, extended response (in 30 μsec.)
1	0	1553A standard, 1553A response (in 9 μsec.)
1	1	1553A standard, extended response (in 21 μsec.)

Table 3-1 MIL-STD-1553A/B Operation: BC Mode

When configured as a MIL-STD-1553A bus controller, the channel will operate as follows:

- Looks for the RT response within 9 μsec.
- Defines all mode codes without data
- defines subaddress 00000 as a mode code

4 Remote Terminal Operation

Chapter 4 describes *EXC-1553PCI/MCH* operation in Remote Terminal (RT) mode. The topics covered in this chapter are:

4.1 Control Registers 4-2
4.1.1 Control Register 4-3
4.1.2 Operational Status Register 4-5
4.1.3 Current Command Block Register 4-6
4.1.4 Interrupt Mask Register 4-6
4.1.5 Pending Interrupt Register 4-7
4.1.6 Interrupt Log List Pointer Register 4-8
4.1.7 BIT Word Register 4-8
4.1.8 Time Tag Register 4-9
4.1.9 RT Descriptor Pointer Register 4-9
4.1.10 1553 Status Word Bits Register 4-10
4.1.11 Illegalization Registers 4-11
4.2 Descriptor Block 4-13
4.2.1 Receive Control Word 4-15
4.2.2 Transmit Control Word 4-16
4.2.3 Mode Code Receive Control Word 4-17
4.2.4 Mode Code Transmit Control Word 4-18
4.2.5 Data Pointer A and B (Mode #0) 4-19
4.2.6 Ping-pong Handshake (Mode #0) 4-21
4.2.7 Broadcast Data Pointer (Mode #0) 4-22
4.3 Data Structures 4-23
4.3.1 Subaddress Receive Data 4-23
4.3.2 Subbaddress Transmit Data 4-24
4.3.3 Mode Code Data 4-25
4.4 RT Circular Buffer Modes 4-27
4.4.1 Mode #1 Operation 4-27
4.4.2 Mode #2 Operation 4-30
4.5 Mode Code and Subaddress 4-33
4.6 Encoder and Decoder 4-35
4.7 RT-to-RT Transfer Compare 4-36
4.8 Terminal Address 4-36
4.9 Reset 4-36
4.10 MIL-STD-1553A/B Operation: RT Mode 4-37

Note The *EXC-1553PCI/MCH* can be configured both as a Remote Terminal and as a Bus Monitor. For more information about this feature see section **5.1 RT/Concurrent Monitor Operation**, on page 5-15.

4.1 Control Registers

The Control registers are read/write unless otherwise stated. All Control registers must be accessed in Word mode. All Control register bits are active high and are reset to 0 unless otherwise stated.

Figure 4-1 below illustrates the Control registers for Remote Terminal mode.

Illegalization Registers (16 registers)	0020-003E H
Reserved	0014-001E H
1553 Status Word Bits Register	0012 H
RT Descriptor Pointer Register	0010 H
Time Tag Register	000E H
BIT Word Register	000C H
Interrupt Log List Pointer Register	000A H
Pending Interrupt Register	0008 H
Interrupt Mask Register	0006 H
Current Command Block Register	0004 H
Operational Status Register	0002 H
Control Register	0000 H

Figure 4-1 Control Registers Map: RT Mode

4.1.1 Control Register

Address: 0000 (H)
Read/Write

Use the Control register to configure the channel for RT operation. To make changes to the RT mode and this register, the STEX bit (Bit 15) must be logic 0.

Bit	Bit Name	Description
15	**STEX**	Start Channel Execution 1 = Initiates channel operation. 0 = Inhibits channel operation. A remote terminal address parity error prevents RT Mode operation regardless of the logical state of this bit. If an RT address parity error exists, bit 03 of the Operational Status Register will be set low and bit 02 of the Operational Status Register will be set high.
14	**SBIT**	Start Channel BIT 1 = Places the channel into the Built-In Test routine. The BIT routine takes 1 msec. to execute and has a fault coverage of 93.4%. If the channel has been started, the host must halt the channel in order to place the channel into the Built-In Test mode (STEX = 0). **Note** If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, SBIT has priority.
13	**Reserved**	Set to 0
12	**BUAEN**	Bus A Enable 1 = Enables Bus A operation. 0 = The channel does not recognize Commands received over Bus A.
11	**BUBEN**	Bus B Enable 1 = Enables Bus B operation. 0 = The channel does not recognize Commands received over Bus B.
10	**Reserved**	Set to 0
09	**PPACK**	Ping-Pong Acknowledge. This read-only bit acknowledges the Ping-Pong operation. The Ping-Pong Enable is acknowledged by transitioning from a logical zero to a logical one, while the Ping-Pong Disable is acknowledged by transitioning from a logical one to a logical zero.
07-08	**RTM[1-0]**	Remote Terminal Mode bits. These two bits determine the RT mode of operation. **RTM[1—0] RT Mode** 0 0 Mode #0 Index or Ping-pong operation 0 1 X Reserved 1 0 Mode #1 Circular buffer 1 operation 1 1 Mode #2 Circular buffer 2 operation
05-06	**Reserved**	Set to 0
04	**BCEN**	Broadcast Enable 1 = Enables the broadcast option for RT Mode. 0 = Enables remote terminal address 31 as a unique remote terminal address.

Control Register

Bit	Bit Name	Description
03	**DYNBC**	Dynamic Bus Control Acceptance. This bit controls the channel's ability to accept the dynamic bus Control mode code. 1 = Allows the channel to respond to a dynamic bus Control mode code with status Word bit 18 set to a logic one. 0 = Prevents the assertion of status Word bit 18 upon reception of the dynamic mode code.
02	**PPEN**	Ping-Pong Enable 1 = Enables the ping-pong buffer feature of the channel and disables the message indexing feature. 0 = Disables the ping-pong feature and enables the message indexing feature.
01	**INTEN**	Interrupt Log Enable 1 = Enables the interrupt logging feature. 0 = Prevents the logging of interrupts.
00	**XMTSW**	Transmit Last Status Word 1 = Allows the channel to automatically execute the Transmit Status Word mode code when configured for MIL-STD-1553A mode operation.

Control Register (Continued)

4.1.2 Operational Status Register

Address: 0002 (H)
Read/Write

The Operational Status register provides pertinent status information for RT Mode and is not reset to 0000 H on reset. Instead the bits A/B_STD, and RTA[4-0] are set to 1.

Bit	Bit Name	Description
11-15	**RTA[4-0]**	Remote Terminal Address Bits. These five bits contain the remote terminal address. The RTA4 bit is the MSB bit, while the RTA0 bit is the LSB bit.
10	**RTAPTY**	Terminal Address Parity Bit. This bit is appended to the remote terminal address bus (RTA[4-0]) to supply odd parity. The channel requires odd parity for proper operation.
09	**MSEL1**	Mode Select 1. In conjunction with Mode Select 0, this bit determines the channel's mode of operation.
08	**MSEL0**	Mode Select 0. In conjunction with Mode Select 1, this bit determines the channel's mode of operation.
		MSEL1 / **MSEL0** / **Mode Of Operation** 0 / 0 / BC Mode 0 / 1 / RT Mode 1 / 0 / BM Mode 1 / 1 / RT/Concurrent Monitor mode
07	**A/B_STD**	Military Standard 1553A or 1553B. This bit determines whether the channel will operate under MIL-STD-1553A or 1553B protocol. 1 = Enables the XMTSW bit (Bit 00 of the Control Register) (1553A). 0 = Automatically allows the channel to operate under the MIL-STD-1553B protocol.
04-06	**Reserved**	These read-only bits are not applicable.
03	**EX**	Channel Executing. This read-only bit indicates whether the channel is presently executing or is idle. 1 = The channel is executing. 0 = The channel is idle.
02	**TAPF**	Terminal Address Parity Fail. Read only. This bit indicates the observance of a terminal address parity error. The channel checks for odd parity. This bit reflects the parity of Operational Status Register bits 10-15.
01	**READY**	Channel Ready. This read-only bit is cleared on reset. 1 = The channel has completed initialization or BIT, and regular operation may begin.
00	**TERACT**	Channel Terminal Active. This read-only bit is cleared on reset. 1 = The channel is presently processing a 1553 message.

Operational Status Register

Note 1. Remote Terminal Address and Parity are checked on start of execution

2. To make changes to the RT Mode and this register, the STEX bit (Bit 15 in the Control Register) must be logic 0.

4.1.3 Current Command Block Register

Address: 0004 (H)
Read only

This 16-bit register contains the last valid 1553 Command processed by the channel.

Bit	Bit Name	Description
00-15	**CC[15-0]**	Current Command. These bits contain the latest valid 1553 Command that was received by the channel. This register is valid 13 μsec. after the TERACT bit (Bit 00 of the Operational Status Register) is set to 0.

Current Command Block Register

4.1.4 Interrupt Mask Register

Address: 0006 (H)
Read/Write

EXC-1553PCI/MCH interrupt architecture allows for the masking of all interrupts. An interrupt is masked if the corresponding bit of this register is set to logic 0. This feature allows the host to temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event.

Bit	Bit Name	Description
12-15	**Reserved**	Set to 0
11	**MERR**	Message Error Interrupt
10	**SUBAD**	Subaddress Accessed Interrupt
09	**BDRCV**	Broadcast Command Received Interrupt
08	**IXEQ0**	Index Equal Zero Interrupt
07	**ILLCMD**	Illegal Command Interrupt
00-06	**Reserved**	Set to 0

Interrupt Mask Register

4.1.5 Pending Interrupt Register

Address: 0008 (H)
Read only

The Pending Interrupt Register is used to identify events that generate interrupts. The assertion of any bit in this register generates an interrupt. A register read of the Pending Interrupt Register will clear all bits.

Bit	Bit Name	Description
12-15	**Reserved**	Ignore on read.
11	**MERR**	Message Error Interrupt. 1 = A message error occurred. The channel can detect Manchester, sync-field, Word count errors (too many or too few), MIL-STD-1553 Word parity, bit count errors (too many or too few), and protocol errors. If not masked, this bit is always set and an interrupt generated when the channel asserts bit-time 9 (Message Error) of the 1553 status Word (e.g., illegal Commands, invalid Data Word, etc.).
10	**SUBAD**	Subaddress Accessed Interrupt. 1 = A pre-selected subaddress has transacted a message. To determine the exact subaddress, the host interrogates the interrupt log IAW.
09	**BDRCV**	Broadcast Command Received Interrupt. 1 = The channel's receipt of a valid broadcast Command. The channel suppresses status Word transmission.
08	**IXEQ0**	Index Equal Zero Interrupt. The channel sets this bit to 1 to indicate the completion of a pre-defined number of Commands by the RT. Upon assertion of this interrupt, the host updates the subaddress descriptor to prevent the potential loss of data.
07	**ILCMD**	Illegal Command Interrupt. 1 = The channel received an illegal Command. Upon receipt of this Command, the channel responds with a status Word only; Bit-time 09 (Message Error) of the 1553 status Word is set to a logic 1.
00-06	**Reserved**	Ignore on read.

Pending Interrupt Register

4.1.6 Interrupt Log List Pointer Register

Address: 000A (H)
Read/Write

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts.

The *EXC-1553PCI/MCH* architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K memory space. The lower 5 bits of this register should be initialized to a logic 0. The channel controls the lower 5 bits to implement the ring-buffer architecture. Read this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Bit	Bit Name	Description
00-15	**ILLP[15-0]**	Interrupt Log List Pointer Bits. **Note** Bits 05-15 indicate the starting Base Address, while bits 00-04 indicate the ring location of the Interrupt Log List

Interrupt Log List Pointer Register

4.1.7 BIT Word Register

Address: 000C (H)
Read/Write

The BIT Word register contains information on the current status of the channel hardware. The RT transmits the contents of the register upon reception of a Transmit BIT Word Mode Code.The user defines the lower 8 bits of this register.

Bit	Bit Name	Description
15	**DMAF**	DMA Fail. 1 = All the channel's internal DMA activity was not completed within 16 μsec.
14	**WRAPF**	Wrap Fail. The channel automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the WRAPF bit is set. The loopback path is via the MIL-STD-1553 bus transceiver.
13	**TAPF**	Terminal Address Parity Fail. This bit reflects the outcome of the remote terminal address parity check. 1 = A parity failure. When a parity error occurs the channel does not begin operation (STEX bit forced to a logic 0) and bus A and B do not enable.
12	**BITF**	BIT Fail. 1 = A BIT failure. Interrogate bits 11 through 08 to determine the specific failure.
11	**BUAF**	Bus A Fail. 1 = A BIT test failure in Bus A.
10	**BUBF**	Bus B Fail. 1 = A BIT test failure in Bus B.
09	**MSBF**	Memory Test Fail. Most significant memory byte failure.
08	**LSBF**	Memory Test Fail. Least significant memory byte failure.
00-07	**UDB[7-0]**	User-Defined Bits.

BIT Word Register

4.1.8 Time Tag Register

Address: 000E (H)
Read Only

The Time Tag register reflects the state of a 16-bit free running counter. The resolution of this counter is 64 μsec./bit. The Time Tag counter is automatically reset when the channel receives a valid synchronize without Data mode code. The channel automatically loads the Time Tag counter with the data associated with reception of a valid synchronize with Data mode code.

The Time Tag counter begins operation in one of two cases:

- *Either* within 64 μsec. of the rising (final) edge of a reset
- *Or* the receipt of one of the following valid mode codes:
  - reset of the remote terminal
  - sync with/without data

When the channel is halted (STEX bit 15 in the Control register = 0), the Time Tag continues to run.

Bit	Bit Name	Description
00-15	**TT[15-0]**	Time Tag Counter Bits.

Time Tag Register

4.1.9 RT Descriptor Pointer Register

Address: 0010 (H)
Read/Write

Each subaddress and mode code has a reserved block of memory containing information about how to process a valid Command to that subaddress or mode code. Located contiguously in memory, these reserved memory locations are called a descriptor space. The RT Descriptor Pointer register contains an address that points to the top of this memory space. The channel uses the T/R bit, subaddress/mode code field, and mode code to select one block in the descriptor table for message processing. The RT Descriptor Pointer register is static during message processing.

Bit	Bit Name	Description
00-15	**RTDA[15-0]**	RT descriptor Address Bits

RT Descriptor Pointer Register

4.1.10 1553 Status Word Bits Register

Address: 0012 (H)
Read/Write

The 1553 Status Word Bits register controls the outgoing MIL-STD-1553 Status Word. The host controls the Instrumentation, Busy, Terminal Flag, Service Request, and Subsystem Flag by writing to bits 09 through 00 of this register. The channel's Status Word response reflects assertion of these bit(s) until negated by the host unless the Immediate Clear Function is enabled. The Immediate Clear Function automatically clears these bits after being transmitted in a Status Word.

The Immediate Clear Function does not affect the operation of the Transmit Last Status Word and Transmit Last Command Word Mode Codes. Transaction of a legal valid Command with the INS bit set to a logic one and the Immediate Clear Function enabled, results in the transmission of a 1553 Status Word with bit 10 asserted. If the ensuing Command is a Transmit Last Status Word or Last Command mode code, bit 10 of the outgoing 1553 Status Word remains a logic 1.

For MIL-STD-1553B applications, the 1553 Status Word Bits register is as follows:

Bit	Bit Name	Description
15	**IMCLR**	Immediate Clear Function. 1 = Enables the Immediate Clear Function (IMF) of the channel. Enabling the IMF results in the clearing of the INS, BUSY, TF, SRQ, and/or SUBF bit immediately after a message is completed. To enable this function, set this bit to 1 when setting bit(s) INS, BUSY, TF, SRQ, and/or SSYSF to 1. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
10-14	**Reserved**	Set to 0
09	**INS**	Instrumentation Bit. This bit sets the Instrumentation bit of the MIL-STD-1553B Status Word. (Bit 10 of the Status Word).
08	**SRQ**	Service Request Bit. This bit sets the Service Request bit of the MIL-STD-1553B Status Word. (Bit 11 of the Status Word).
04-07	**Reserved**	Set to 0
03	**BUSY**	Busy Bit. Assertion of this bit is reflected in the outgoing MIL-STD-1553B Status Word. 1 = Prevents memory accesses. (Bit 16 of the Status Word).
02	**SSYSF**	Subsystem Flag Bit. This bit sets the Subsystem Flag bit of the MIL-STD-1553B Status word. (Bit 17 of the Status Word).
01	**Reserved**	Set to 0
00	**TF**	Terminal Flag. Assertion of this bit is reflected in the outgoing MIL-STD-1553B Status Word. The channel automatically sets this bit if a BIT failure occurs. Inhibit Terminal Flag mode code prevents the assertion by the host. Override Inhibit Terminal Flag Mode Code re-establishes the Terminal Flag option. (Bit 19 of the Status Word).

1553 Status Word Bits Register: MIL-STD-1553B

For MIL-STD-1553A applications, the 1553 Status Word Bits register.

Bit	Bit Name	Description
15	**IMCLR**	Immediate Clear Function. 1 = Enables the Immediate Clear Function (IMF) of the channel. Enabling the IMF results in the clearing of the bits 10-19 immediately after a Status Word is transmitted. To enable this function, set this bit when writing to bits 10-19. This bit should be used consistently since once set, it will remain set, and once cleared, it will remain cleared.
10-14	**Reserved**	Set to 0
09	**SB10**	Status bit time 10
08	**SB11**	Status bit time 11
07	**SB12**	Status bit time 12
06	**SB13**	Status bit time 13
05	**SB14**	Status bit time 14
04	**SB15**	Status bit time 15
03	**SB16**	Status bit time 16
02	**SB17**	Status bit time 17
01	**SB18**	Status bit time 18
00	**SB19**	Status bit time 19

1553 Status Word Bits Register: MIL-STD-1553A

4.1.11 Illegalization Registers

Address: 0020 – 003E (H)

The 16 registers are divided into eight blocks, two registers per block, as shown in Table 4-1:

Block Name	Address (H)
Receive	0020 and 0022
Transmit	0024 and 0026
Broadcast Receive	0028 and 002A
Broadcast Transmit (Automatically Illegalized)	002C and 002E
Mode Code Receive	0030 and 0032
Mode Code Transmit	0034 and 0036
Broadcast Mode Code Receive	0038 and 003A
Broadcast Mode Code Transmit	003C and 003E

Table 4-1 Illegalization Register Blocks

The blocks correspond to the following types of Commands. Register address 0020 (H) and 0022 (H) illegalize receive Commands to 32 subaddresses. The most significant bit of register 0020 (H) controls the illegalization of subaddress 01111. The least significant bit controls subaddress 00000. Register 0022 (H) controls

illegalization of subaddresses 10000 through 11111. The least significant bit relates to subaddress 10000; the most significant bit relates to subaddress 11111. Transmit Commands and Broadcast Commands (both receive and transmit) use the same encoding scheme as receive subaddress illegalization.

Register 0030 (H) through 003E (H) controls the illegalization of mode codes. Register 0030 (H) governs the illegalization of receive mode codes (T/R bit = 0) 00000 through 01111 and register 0032 (H) mode codes 10000 through 11111. Register blocks Transmit Mode Code (T/R bit = 1), Broadcast Receive Mode Codes, and Broadcast Transmit Mode Codes use the same decode scheme as receive mode codes.

Table 4-2 shows the illegalization register map. For Receive, Transmit, Broadcast Receive, and Broadcast Transmit blocks, the numbers shown in the column under each bit number identify the specific subaddress or mode code (in hex) that the register bit illegalizes (Logical 0 = legal, Logical 1 = illegal).

Name	Register Address (H)																
Bit #		**15**	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
Receive	0020	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0022	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Transmit	0024	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0026	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Broadcast Receive	0028	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	002A	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Broadcast Transmit	002C	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
	002E	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX	XX
Mode Code Receive	0030	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0032	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Code Transmit	0034	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	0036	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Broadcast Receive	0038	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	003A	1F	1E	1D	1C	1B	1A	19	18	17	16	15	14	13	12	11	10
Mode Broadcast Transmit	003C	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
	003E	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY	YY

Table 4-2 Illegalization Register Map

1. XX = Automatically illegalized by the channel.
2. YY = Automatically illegalized by the channel in 1553B only.
3. ZZ = Automatically illegalized by the channel in 1553B and 1553A if XMTSW is enabled.
4. WW = Automatically illegalized in 1553A.
5. UU = Automatically illegalized in 1553A if XMTSW enabled.

4.2 Descriptor Block

To process messages, the channel uses data from the Control Registers with data stored in the RAM. The channel accesses a 4-word descriptor block stored in RAM. The descriptor block is accessed at the beginning and end of Command processing. Multiple descriptor blocks are sequentially entered into memory to form a descriptor table. The following paragraphs discuss the descriptor block in detail.

The host controlling the channel allocates 512 consecutive memory spaces for the subaddress and mode code Descriptor Table (see Figure 4-2, page 4-14). The top of the Descriptor Table can reside at any address location. The Control registers are linked to the descriptor table via the Descriptor Address Register contents. Each descriptor block contains a Control Word, Data Pointer A, Data Pointer B, and Broadcast Data Pointer. Each subaddress and mode code is assigned a descriptor for receive and transmit Commands (T/R bit equals 0 or 1.).

Control Word information allows the channel to generate interrupts, buffer messages, and control message processing. For a receive Command, the Data List Pointer is read to determine the top of the data buffer. The channel stores data sequentially from the top of data buffer plus two locations (e.g., 0100H, 0102H, 0104H, 0106H, etc.). When processing a transmit Command, the Data List Pointer is read to determine where Data Words are retrieved. The channel retrieves Data Words sequentially from the address the Data List Pointer designates plus two 16-bit address locations.

The Broadcast Data Pointer allows for separate storage of non-broadcast data from broadcast data per MIL-STD-1553B Notice II. The user enables or disables this feature via the Control Word's least significant bit. When disabled, the non-broadcast and broadcast data is stored via Data List Pointer A or B. For transmit Commands, the Broadcast Data Pointer is not used. The channel does not transmit any information on the receipt of a broadcast transmit Command.

The channel reads the descriptor block during Command processing (i.e., after assertion of TERACT). The channel reads the Control Word and three Data Pointers. The channel then begins the acquisition of Data Words for either transmission or storage.

After transmission or reception, the channel begins post-processing. The Descriptor Block is updated. An optional interrupt log entry is performed after a descriptor update. During the descriptor update, the channel modifies the Control Word index field and bits 4, 2, and 1, if required. The channel updates Data Pointer A if no message errors occurred during the message transaction. Reception of a broadcast Command, with no message errors, results in the update of the Broadcast Data Pointer. Neither Data Pointer A or B is updated if the channel has the ping-pong mode of operation enabled.

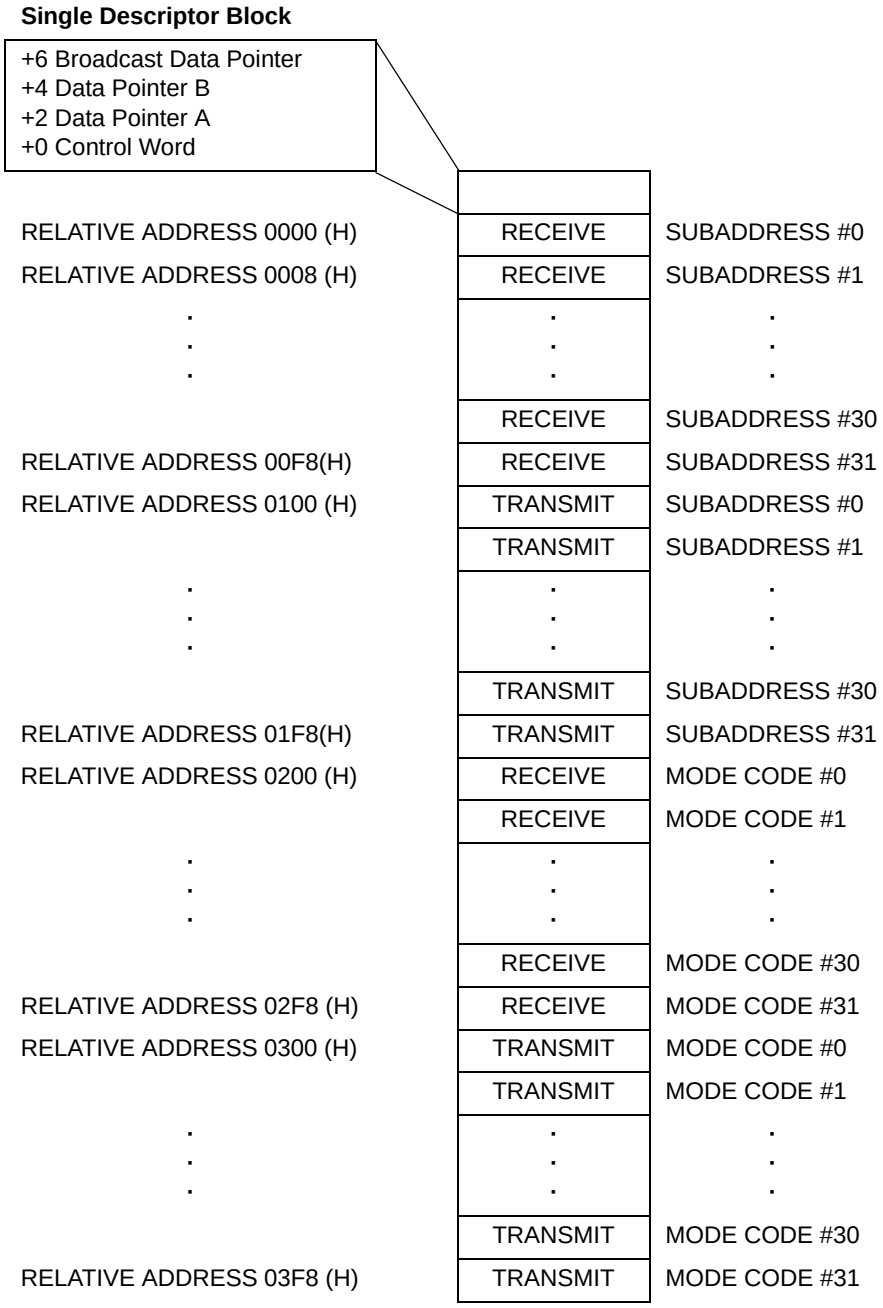

Single Descriptor Block
+6 Broadcast Data Pointer
+4 Data Pointer B
+2 Data Pointer A
+0 Control Word
RELATIVE ADDRESS 0000 (H) RECEIVE SUBADDRESS #0
RELATIVE ADDRESS 0008 (H) RECEIVE SUBADDRESS #1
RECEIVE SUBADDRESS #30
RELATIVE ADDRESS 00F8(H) RECEIVE SUBADDRESS #31
RELATIVE ADDRESS 0100 (H) TRANSMIT SUBADDRESS #0
TRANSMIT SUBADDRESS #1
TRANSMIT SUBADDRESS #30
RELATIVE ADDRESS 01F8(H) TRANSMIT SUBADDRESS #31
RELATIVE ADDRESS 0200 (H) RECEIVE MODE CODE #0
RECEIVE MODE CODE #1
RECEIVE MODE CODE #30
RELATIVE ADDRESS 02F8 (H) RECEIVE MODE CODE #31
RELATIVE ADDRESS 0300 (H) TRANSMIT MODE CODE #0
TRANSMIT MODE CODE #1
TRANSMIT MODE CODE #30
RELATIVE ADDRESS 03F8 (H) TRANSMIT MODE CODE #31

Figure 4-2 Descriptor Table

4.2.1 Receive Control Word

Information contained in the Receive Control Word assists the channel in message processing. The following bits describe the receive subaddress descriptor Control Word. The descriptor Control Word is initialized by the host and updated by the channel during Command post-processing.

Bit	Bit Name	Description
08-15	**INDX**	Index Field. These bits define multiple message buffer length. The host uses this field to instruct the channel to buffer *N* messages. *N* can range from 0 (00 H) to 256 (FF H). If buffer ping-ponging is enabled, the INDX field is 'don't care' (i.e., does not contain applicable information). During ping-pong mode operation, you should initialize the index field to 00 (H). The RT does not perform multiple message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the subaddress is illegalized. The channel can generate an interrupt when the index field transitions from one to zero (see bit 07).
07	**INTX**	Interrupt Index Equals Zero. 1 = Enables the generation of an interrupt when the index field transitions from 1 to 0. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
06	**IWA**	Interrupt When Accessed. 1 = Enables the generation of an interrupt when the subaddress receives a valid Command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	**IBRD**	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when the subaddress receives a valid broadcast Command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	**BAC**	Block Accessed. The host initializes this bit to zero; the channel overwrites the zero with a logic one upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	**Reserved**	Set to 0
02	**A/B**	Buffer A/B. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a 'don't care' if buffer ping-ponging is not enabled.
01	**BRD**	Broadcast Received. 1 = Reception of a valid broadcast Command.
00	**NII**	Notice II. 1 = Enables the use of the Broadcast Data Pointer as a buffer for Broadcast Command information. 0 = Broadcast information is stored in the same buffer as non-broadcast information.

Receive Control Word

4.2.2 Transmit Control Word

Information contained in the Transmit Control Word assists the *EXC-1553PCI/MCH* in message-processing. The following bits describe the transmit subaddress descriptor Control Word. The descriptor control Word is initialized by the host and updated by the channel during Command post-processing.

Bit	Bit Name	Description
07-15	**Reserved**	Set to 0
06	**IWA**	Interrupt When Accessed. 1 = Enables the generation of an interrupt when the subaddress receives a valid Command. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	**Reserved**	Set to 0
04	**BAC**	Block Accessed. The host initializes this bit to zero; the channel overwrites the zero with a logic one upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	**Reserved**	Set to 0
02	**A/B**	Buffer A/B. Indicates the Data pointer to access when buffer ping-pong is enabled. During initialization, the host designates the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a ‘don’t care’ if buffer ping-ponging is not enabled.
01	**BRD**	Broadcast Received. 1 = Reception of a Broadcast Command.
00	**Reserved**	Set to 0

Transmit Control Word

4.2.3 Mode Code Receive Control Word

Information contained in the Mode Code Receive Control Word assists the *EXC-1553PCI/MCH* in message processing. The following bits describe the receive mode code descriptor Control Word. The descriptor control Word is initialized by the host and updated by the channel during Command postprocessing.

Note In MIL-STD-1553A, all mode codes are without data, and the T/R bit is ignored.

Bit	Bit Name	Description
08-15	**INDX**	Index Field. These bits define multiple message buffer length. The host uses this field to instruct the channel to buffer *N* messages. *N* can range from 0 (00 H) to 256 (FF H). If buffer ping-ponging is enabled, the INDX field is 'don't care' (i.e., does not contain applicable information). The channel does not perform message buffering in the ping-pong mode of operation. The index decrements each time a complete message is transacted (no message errors). The index does not decrement if the mode code is illegalized. The channel can generate an interrupt when the index field transitions from one to zero (see bit 07).
07	**INTX**	Interrupt Index Equals 0. 1 = Enables the generation of an interrupt when the index field transitions from 1 to 0. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
06	**IWA**	Interrupt When Accessed. 1 = Enables the generation of an interrupt when mode code Command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	**IBRD**	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when a valid broadcast mode code Command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	**BAC**	Block Accessed. The host initializes this bit to zero; the channel overwrites the zero with a logic 1 upon completion of message processing. Upon reading a one, the host resets this bit to zero in preparation for the next message.
03	**Reserved**	Set to 0
02	**A/B**	Buffer A/B. Indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, you designate the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a 'don't care' if buffer ping-ponging is not enabled.
01	**BRD**	Broadcast Received. 1 = Reception of a valid broadcast Command.
00	**NII**	Notice II. 1 = Enables the use of the Broadcast Data Pointer as a buffer for broadcast Command information. 0 = Broadcast information is stored in the same buffer as non-broadcast information.

Mode Code Receive Control Word

4.2.4 Mode Code Transmit Control Word

Information contained in the Mode Code Transmit Control Word assists the *EXC-1553PCI/MCH* in message processing. The following bits describe the transmit mode code descriptor Control Word. You initialize the descriptor Control Word and the channel updates it during Command post-processing.

Note In MIL-STD-1553A, all mode codes are without data, and the T/R bit is ignored.

Bit	Bit Name	Description
07-15	**Reserved**	Set to 0
06	**IWA**	Interrupt When Accessed. 1 = Enables the generation of an interrupt when mode code Command is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
05	**IBRD**	Interrupt Broadcast Received. 1 = Enables the generation of an interrupt when a broadcast mode code is received. The interrupt is entered into the Pending Interrupt Register if not masked in the Mask Register. An interrupt is generated after message processing.
04	**BAC**	Block Accessed. The host initializes this bit to 0; the channel overwrites the 0 with a logic 1 upon completion of message processing. Upon reading a 1, the host resets this bit to 0 in preparation for the next message.
03	**Reserved**	Set to 0
02	**A/B**	Buffer A/B. This bit indicates the last buffer accessed when buffer ping-pong is enabled. During initialization, you designate the first buffer used by setting this bit. 1 = Buffer A 0 = Buffer B This bit is a ‘don’t care’ if buffer ping-ponging is not enabled.
01	**BRD**	Broadcast Received. 1 = Reception of a broadcast Command.
00	**Reserved**	Set to 0

Mode Code Transmit Control Word

4.2.5 Data Pointer A and B (Mode #0)

Data List Pointer A and B contains address information for the retrieval and storage of message Data Words. In the index mode of operation, the channel reads Data Pointer A to determine the location of data for retrieval or storage. The channel uses the Data Pointer to initialize an internal counter, which increments after each Data Word. For a receive Command, the channel stores the incoming Data Word sequentially into memory. As part of Command post-processing, the channel writes a new Data pointer into the descriptor block. The channel continues to update the Data pointer until the Control Word index field decrements to zero. An example is shown in **Figure 4-3 RT Non-broadcast Receive Message Indexing**, on page 4-20. The index feature is not applicable for transmit Commands (i.e., T/R bit = 1).

Bit	Bit Name	Description
00-15	**DP[15-0]**	Data Pointer Bits. The second and third Words of the descriptor block contain the data buffer location. The channel accesses either Data Pointer A or Data Pointer B depending on the state of Control Word Bit 02 during ping-pong operation. For index operation, the channel accesses only Data Pointer A. The channel updates Data pointer A after message processing is complete and the index field is not equal to zero and ping-pong operation disabled. Bit 15 is the most significant bit; bit 00 is the least significant bit.

Data Pointer A and B

For ping-pong buffer operation, the host uses either Data Pointer A or Data Pointer B. The channel determines which pointer to access via the state of Control Word bit 02. The channel retrieves or stores Data Words from the address contained in the Data pointer, automatically incrementing the Data Pointer as Data Words are received. The Data pointer is never updated as part of Command postprocessing in the ping-pong mode of operation. See Figures 4-4 and 4-5.

Receive Address	CONTROL WORD	Index Field Contents 03xx (H)
# Descriptor Block	DATA POINTER A	Data Pointer A: 0100 (H)
	DATA POINTER B	Data Pointer B: Xxxx (H)
	BROADCAST DATA POINTER	Broadcast Data Pointer: Xxxx (H)
Command #1 Receive three words	Message Info Word	0200 (H) Index equals three
	Time Tag	0202 (H)
	Data Word #1	0204 (H)
	Data Word #2	0206 (H)
	Data Word #3	0208 (H) Index decrements two
Command #2 Receive two words	Message Info Word	020A(H) Index equals two
	Time Tag	020C (H)
	Data Word #1	020E (H)
	Data Word #2	0210(H) Index decrements to one
Command #3 Receive three words	Message Info Word	0212 (H) Index equals one
	Time Tag	0214 (H)
	Data Word #1	0216 (H)
	Data Word #2	0218(H)
	Data Word #3	021A (H) Index decrements to zero
		[Data pointer A updated to 010e (H), interrupt generated enabled]

Figure 4-3 RT Non-broadcast Receive Message Indexing

X = don't care

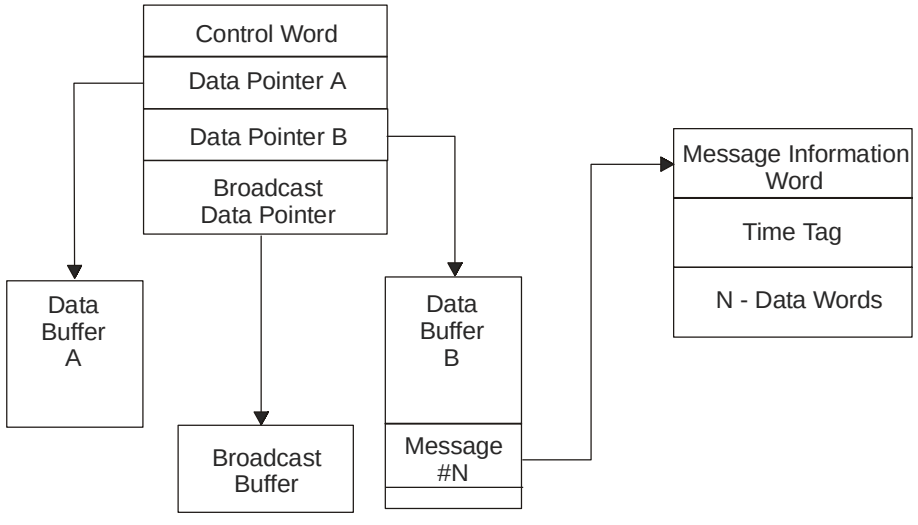


Figure 4-4 *EXC-1553PCI/MCH* Descriptor Block – Receive

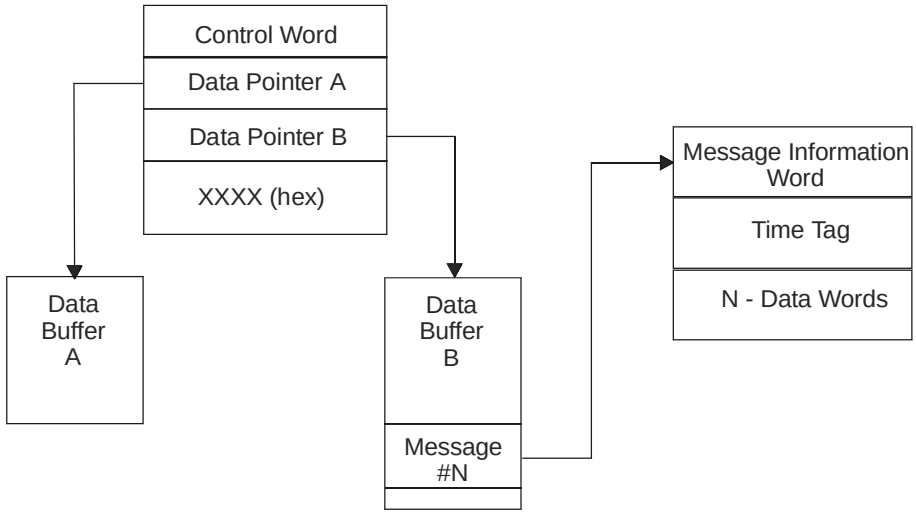


Figure 4-5 *EXC-1553PCI/MCH* Descriptor Bock – Transmit

4.2.6 Ping-pong Handshake (Mode #0)

The *EXC-1553PCI/MCH* provides a mechanism to enable and disable buffer ping-pong operation. If ping-pong is enabled during Remote Terminal operation, data will be stored/retrieved in alternative buffers each time a new message is processed. If ping-pong is disabled a single buffer will be used for all message processing.

The Handshake mechanism operates as follows:

Prior to starting Remote Terminal operation, enable the buffer ping-pong feature by writing a logical 1 to bit 02 of the Control Register. During ping-pong operation, the remote terminal ping-pongs between the two data buffers, for each subaddress or mode code, on a message-by-message basis. Each unique MIL-STD-1553 subaddress and mode code is assigned two data buffer locations (A and B). The remote terminal retrieves data from a buffer or stores data into a buffer depending on the message type (i.e., transmit or receive Command). During ping-pong operation, the Remote Terminal determines the active subaddress or mode code buffer at the beginning of message processing, the remote terminal complements bit 02 of the Descriptor Control Word to access the alternate buffer on the following message (i.e., ping-pong).

The application software disables ping-pong operation by writing a logical 0 to Control Register bit 02. The disable of ping-pong operation is acknowledged by bit 09 of the Control Register. Bit 09 of the Control Register acknowledges the ping-pong disable by transitioning from a logical 1 to a logical 0. The application software interrogates bit 02 of each Descriptor Control Word to determine the active buffer on a subaddress or mode code basis. If bit 02 is a logical 0, the remote terminal uses Buffer A and the application software off-loads or loads Buffer A.

The application software enables ping-pong operation by writing a logical 1 to Control Register bit 02. The enable of ping-pong operation is acknowledged by bit 09 of the Control Register. Bit 09 of the Control Register acknowledges the ping-pong enable by transitioning from a logical 0 to a logical 1.

4.2.7 Broadcast Data Pointer (Mode #0)

The Broadcast Data Pointer contains the address for the Message Information Word, Time Tag Word, and Data Words associated with a broadcast Command. The following bits describe the receive subaddress/mode code descriptor Broadcast Data Pointer. If ping-pong operation is disabled, the channel automatically increments this Data Pointer during Command post-processing,

Bit	Bit Name	Description
00-15	**BP[15-0]**	Broadcast Data Pointer. The fourth Word of the descriptor block contains the broadcast data buffer location. This pointer can reside anywhere in memory space. The channel accesses this pointer when Control Word bit 00 is a logic 1 and broadcast is enabled. Bit 15 is the most significant bit, bit 00 is the least significant bit. **Note** 1. If ping-pong is enabled, this pointer does not update. 2. When the broadcast Command is followed by a Transmit Last Command or Last Status Word mode code, the channel transmits a Status Word with bit 15 of the Status Word set to a logic 1. The broadcast bit is cleared when the next valid non-Broadcast Command is received.

Broadcast Data Pointer

4.3 Data Structures

The following sections discuss the Data structures that result from Command processing. For each complete message processed, the *EXC-1553PCI/MCH* generates a Message Information Word and Time Tag Word. These Words aid the host in further message processing. The Message Information Word contains Word count, message type, and message error information. The Time Tag Word is a 16-bit Word containing the Command validity time. The Time Tag Word data comes from the channel's internal Time Tag counter.

4.3.1 Subaddress Receive Data

For receive Commands, the channel stores Data Words plus two additional Words. The channel adds a Receive Information Word and Time Tag Word to each receive Command data packet. The channel places the Receive Information Word and Time Tag Word ahead of the Data Words associated with a receive Command (see Figures 4-3, 4-4 and4-5 above). When message errors occur, the channel stores the Receive Information Word and Time Tag Word. Once a message error condition is observed, all Data Words are considered invalid.

Data storage occurs at the memory location pointed to by the Data pointer plus two 16-bit locations.

Bit	Bit Name	Description
11-15	**WC[4-0]**	Word Count Bits. These five bits contain Word count information extracted from the Command Word bits 15 to 19.
10	**Reserved**	Ignore on read.
09	**BUA/B**	Bus A/B. 1 = The message was received on Bus A. 0 = The message was received on Bus B.
08	**RTRT**	Remote Terminal to Remote Terminal Transfer. The Command processed was an RT-to-RT transfer.
07	**ME**	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	**Reserved**	Ignore on read.
04	**ILL**	Illegal Command Received. 1 = The Command received was an illegal Command.
03	**TO**	Time-Out Error. 1 = The channel did not receive the proper number of Data Words, i.e., the number of Data Words received was less than the Word count specified in the Command Word.
02	**OVR**	Overrun Error. 1 = The channel received a Word when none was expected or the number of Data Words received was greater then expected.
01	**PRTY**	Parity Error. 1 = The channel observed a parity error in the incoming Data Words.
00	**MAN**	Manchester Error. 1 = The channel observed a Manchester error in the incoming Data Words.

Receive Information Word

4.3.2 Subbaddress Transmit Data

The user is responsible for organizing the data packet (i.e., *N* Data Words) into memory and establishing the applicable Data Pointer. The user can allocate two 16-bit memory locations at the top of the data packet for the storage of the Transmit Information Word and the Time Tag Word. An example transmit Data structure for three Words is shown below:

Data Pointer A ⟶	0200 (H)	XXXX	Reserved for Transmit Info Word
equals 0100 (H)	0202 (H)	XXXX	Reserved for Time Tag Word
	0204 (H)	FFFF	Data Word #1
	0206 (H)	FFFF	Data Word #2
	0208 (H)	FFFF	Data Word #3

Note Data pointer A points to the top of the Data structure, not to the top of the Data Words.

Bit	Bit Name	Description
11-15	**WC[4-0]**	Word Count Bits. These five bits contain Word count information extracted from the Command Word bits 15 to 19.
10	**Reserved**	Ignore on read.
09	**BUA/B**	Bus A/B. 1 = The message was received on Bus A. 0 = The message was received on Bus B.
08	**Reserved**	Ignore on read.
07	**ME**	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for more detail.
05-06	**Reserved**	Ignore on read.
04	**ILL**	Illegal Command Received. 1 = The Command received was an illegal Command.
03	**Reserved**	Ignore on read.
02	**OVR**	Overrun Error. 1 = The channel received a Data Word with a Transmit Command.
00-01	**Reserved**	Ignore on read.

Transmit Information Word

4.3.3 Mode Code Data

The Transmit and Receive Data Structures for mode codes are similar to those for a subaddress. The receive Data structure contains an Information Word, Time Tag Word, and message Data Word. All receive mode codes with data have one associated Data Word. Data storage occurs at the memory location pointed to by the Data pointer plus two 16-bit locations. Reception of the synchronize with Data mode code automatically loads the Time Tag counter and stores the Data Word at the address defined by the Data pointer plus two 16-bit locations.

The transmit mode code Data structure contains an Information Word, Time Tag Word, and associated Data Word. The host is responsible for linking the channel Data Pointer to the data (e.g., Transmit Vector Word). For mode codes with internally generated Data Words (e.g., Transmit BIT Word, Transmit Last Command), the transmitted Data Word is added to the Data structure.

For MIL-STD-1553A mode of operation, all mode codes are defined without Data Words. For mode codes without data, the Data structure contains the Message Information Word and Time-Tag Word only.

Note In MIL-STD-1553A all mode codes are without data and the T/R bit is ignored.

Mode Code Receive Information Word

Bit	Bit Name	Description
11-15	**MC[4-0]**	Mode Code. These five bits contain the mode code information extracted from the receive Command Word bits 15 to 19.
10	**Reserved**	Ignore on read.
09	**BUA/B**	Bus A/B. 1 = The message was received on Bus A. 0 = The message was received on Bus B.
08	**RTRT**	Remote Terminal to Remote Terminal Transfer. 1 = The Command processed was an RT-to-RT transfer.
07	**ME**	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	**Reserved**	Ignore on read.
04	**ILL**	Illegal Command Received. 1 = The Command received was an illegal Command.
03	**TO**	Time-out Error. 1 = The channel did not receive the proper number of Data Words, i.e., the number of Data Words received was less than the Word count specified in the Command Word.
02	**OVR**	Overrun Error. 1 = The channel received a Word when none was expected, or the number of Data Words received was greater than expected.
01	**PRTY**	Parity Error. 1 = The channel observed a parity error in the incoming Data Words.
00	**MAN**	Manchester Error. 1 = The channel observed a Manchester error in the incoming Data Words.

Mode Code Transmit Information Word

Bit	Bit Name	Description
11-15	**MC[4-0]**	Mode Code. These five bits contain the mode code information extracted from the Command Word bits 15 to 19.
10	**Reserved**	Ignore on read.
09	**BUA/B**	Bus A/B. 1 = The message was received on Bus A. 0 = The message was received on Bus B.
08	**Reserved**	Ignore on read.
07	**ME**	Message Error. 1 = A message error condition was observed during processing. See bits 00 to 04 for details.
05-06	**Reserved**	Ignore on read.
04	**ILL**	Illegal Command Received. 1 = The Command received was an illegal Command.
03	**Reserved**	Ignore on read.
02	**OVR**	Overrun Error. 1 = The channel received a Data Word with a Transmit Command.
00-01	**Reserved**	Ignore on read.

4.4 RT Circular Buffer Modes

The RT circular buffer modes simplify the software service of remote terminals implementing bulk or periodic data transfers. Select the preferred mode at start-up by writing to Control Register bits 07 and 08 (see **Control Register**, on page 4-3). The two modes, Mode #1 and Mode #2 are discussed in sections 4.4.1 and 4.4.2

4.4.1 Mode #1 Operation

In this mode the channel merges transmit or receive data into a circular buffer along with message information.

For each valid receive message, the channel enters a message information Word, Time-Tag Word, and Data Word(s) into a unique receive circular buffer.

For each valid transmit message, the channel enters a message information Word and Time Tag Word into reserved memory locations within the transmit circular buffer. The channel automatically controls the wrap around of circular buffers.

4.4.1.1 MODE #1 DESCRIPTOR BLOCK

Each subaddress and mode code both transmit and receive, has a unique circular buffer assignment. The channel decodes the Command Word T/R bit, subaddress/ mode code field, and Word_count/mode_code field to select a unique descriptor block that contains Control Word, TA, CA, and BA (see **Figure 4-6 RT Mode #1 Descriptor Block And Circular Buffer**, on page 4-29).

To implement Circular Buffer 1's architecture, the 4-word descriptor block and Control Register are different than in the Mode #0. Bits 15 through 08 of the Control Word are 'don't care'. The second Word of the descriptor block defines the buffer's starting or top address (TA). The TA pointer remains static during message processing. The fourth entry into the descriptor block identifies the buffer's bottom address (i.e., BA) and remains static during message processing. The third descriptor block Words represent the current address (i.e., CA) in the buffer and is dynamic. If the channel observes no message error conditions, the CA pointer updates at the end of message processing. The application software reads the dynamic CA pointer to determine the current bottom of the buffer.

The TA (top of buffer) and BA (bottom of buffer) pointers define the circular buffer's length. The CA pointer identifies the current address (i.e., last accessed address plus one). The circular buffer wraps to the top address after completing a message that results in CA being greater than or equal to BA. If CA increments past BA during intra-message processing, the channel will access memory (read or write) address locations past BA. Delimit all circular buffer boundaries with at least 34 address locations.

Note In this mode of operation, bits INDX, NII and A/B of the Descriptor Control Word and the PPEN bit of the Control Register are 'don't care'.

4.4.1.2 MODE #1 CIRCULAR BUFFER — RECEIVE MESSAGE PROCESSING

The channel begins all message processing by reading a unique descriptor block after reception and validation of a subaddress or mode code Command Word. The channel internally increments the CA pointer to store the receive Data Word(s). After message processing completes, the channel stores the Message Information Word and Time-Tag Word into the circular buffer preceding the message data. At the end of message processing, the channel updates CA (if no errors detected). For CA larger than BA storage of next message begins at the address location pointed to by the TA pointer, and CA is made equal to TA. If CA is less than BA, CA points to the next available memory location in the buffer (i.e., CA+1).

For transmit Commands, the channel begins transmission of data from memory location CA+2. Reserve the first two locations for the message information Word and Time Tag Word. After message processing completes, the channel enters the message information Word and Time Tag Word into the circular buffer. At the end of message processing, the channel updates CA (if no errors detected). For CA larger than BA, storage of the next message begins at the address location pointed to by the TA pointer, and CA is made to equal TA. If CA is less than BA, CA points to the next available memory location in the buffer (i.e., CA+1).

Note In this mode the Message Information Word bit 5 reflects the reception of broadcast message via the BRD bit.

The channel generates a circular buffer empty/full interrupt when the buffer reaches the end (i.e., CA greater than BA) and begins a new message at the top of the buffer. Bit 08 of the Mask Register and bit 07 of the Descriptor Control Word mask enables the generation of the Full/Empty interrupt.

Figure 4-6 describes the relationship between The top address (TA), bottom address (BA) and current address (CA):

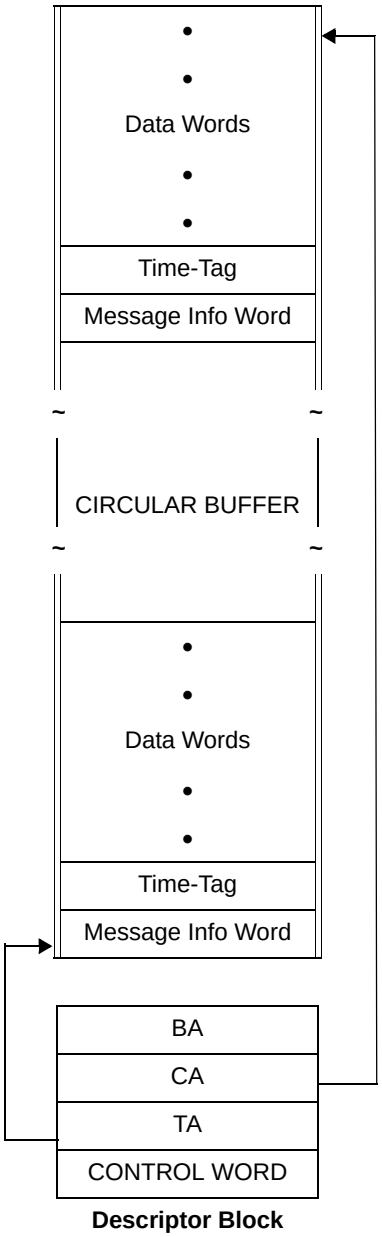


Figure 4-6 RT Mode #1 Descriptor Block And Circular Buffer

4.4.2 Mode #2 Operation

In this mode, the channel separates message data and message information into unique circular buffers. The separation of data from message information simplifies the software that loads and unloads data from the buffers. The message information buffer contains Time-Tag and Message Information Words for each message transacted on the bus, while the data buffer contains the message Data Words. After processing a pre-determined number of messages, both buffers wrap-around.

4.4.2.1 MODE #2 DESCRIPTOR BLOCK

Each subaddress and mode code, both transmit and receive, has a unique pair of circular buffers. The channel decodes the Command Word T/R bit, subaddress/ mode field, and Word_count/mode_code field to select a unique descriptor block that contains Control Word, TA, CA, and MIB (see **Figure 4-7 RT Mode #2 Descriptor Block**, on page 4-32).

To implement Circular Buffer 2's architecture, the descriptor block and Control Register are different than in Mode #0. Bits 15 through 08 of the Control Word specify the Message Information Buffer (MIB) length; the maximum MIB size is 256. Table 4-3 shows how the Control Word's most significant bits select the depth of the MIB. The Control Words eight most significant bits remain static during message processing.

The second Word of the description block defines the top address (TA) of the Data circular buffer. The TA pointer remains static during message processing. The third descriptor Word identifies the current address (i.e., CA) of the Data circular buffer. The application software reads the dynamic CA pointer to determine the current address of the Data buffer. The channel increments the CA pointer, at the end of message processing, until the MIB buffer is full. When the MIB wraps around, the SμMMIT loads the CA pointer with the TA pointer.

The fourth Word in the descriptor block defines the top or base address of the Message Information Buffer (i.e., MIB) and the current MIB address (i.e., offset from base address). The SμMMIT enters the message information Word and Time-Tag Word into the MIB, for each message, until the end of the MIB is reached. When the MIB reaches the end, the next message's message information Word and Time-Tag Word is entered at the top of the MIB. The MIB pointer is a semi-static pointer. The channel updates the current address field at the end of message processing. The Base Address field remains static.

Note In this mode of operation, bits INDX, NII and A/B of the descriptor Control Word and the PPEN bit of the Control Register are 'don't care'.

4.4.2.2 MODE #2 CIRCULAR BUFFER — RECEIVE MESSAGE PROCESSING

The channel begins all message processing by reading the descriptor block of the subaddress or mode code Command received (i.e., Control Word, TA, CA, and MIB). The channel begins storage of Data Word(s) starting at the location contained in the CA pointer. The channel automatically updates the CA pointer internally as message processing progresses. The channel stores the message information Word and Time-Tag Word into the MIB, after receiving the correct number of Data Words, At the end of message processing, the channel updates CA and the MIB Current Address Field (CAF). If CAF equals the specified MIB length, CA is updated to TA and the MIB CAF is reset to zero. If CAF is less than the specified MIB length, CA and MIB CAF point to the next available memory location in each buffer. Control Word bits 15 to 08 specify the MIB length.

For transmit Commands, the channel begins transmission of data from memory location CA. After message processing completes, the channel enters the message information Word and Time Tag Word into the MIB. At the end of message processing, the channel updates CA and the MIB CAF. If CAF equals the specified MIB length, CA is updated to TA and the MIB CAF is reset to zero. If CAF is less than the specified MIB length, CA and MIB CAF point to the next available memory location in each buffer.

Note In this mode the BRD bit is added to the Message Information Word bit 05.

The channel generates a circular buffer empty/full interrupt when the MIB reaches the end and begins a new message at the top of the buffer. Bit 08 of the Mask Register and bit 07 of the Descriptor Control Word mask enable the generation of the Full/Empty interrupt.

Control Word Bits 8-15	Length of MIB (messages)	MIB Pointer Structure (Base and CAF)
FF	128	8 Bit Base Address +8 Bit Current Address Field
7F	64	9 Bit Base Address +7 Bit Current Address Field
3F	32	10 Bit Base Address +6 Bit Current Address Field
1F	16	11 Bit Base Address +5 Bit Current Address Field
0F	8	12 Bit Base Address +4 Bit Current Address Field
07	4	13 Bit Base Address +3 Bit Current Address Field
03	2	14 Bit Base Address +2 Bit Current Address Field
01	1	15 Bit Base Address +1 Bit Current Address Field

Table 4-3 RT Mode #2 Control Word and MIB Pointer Structure

Figure 4-7 describes the relationship between the top address (TA), current address (CA) and Message Information Buffer (MIB):

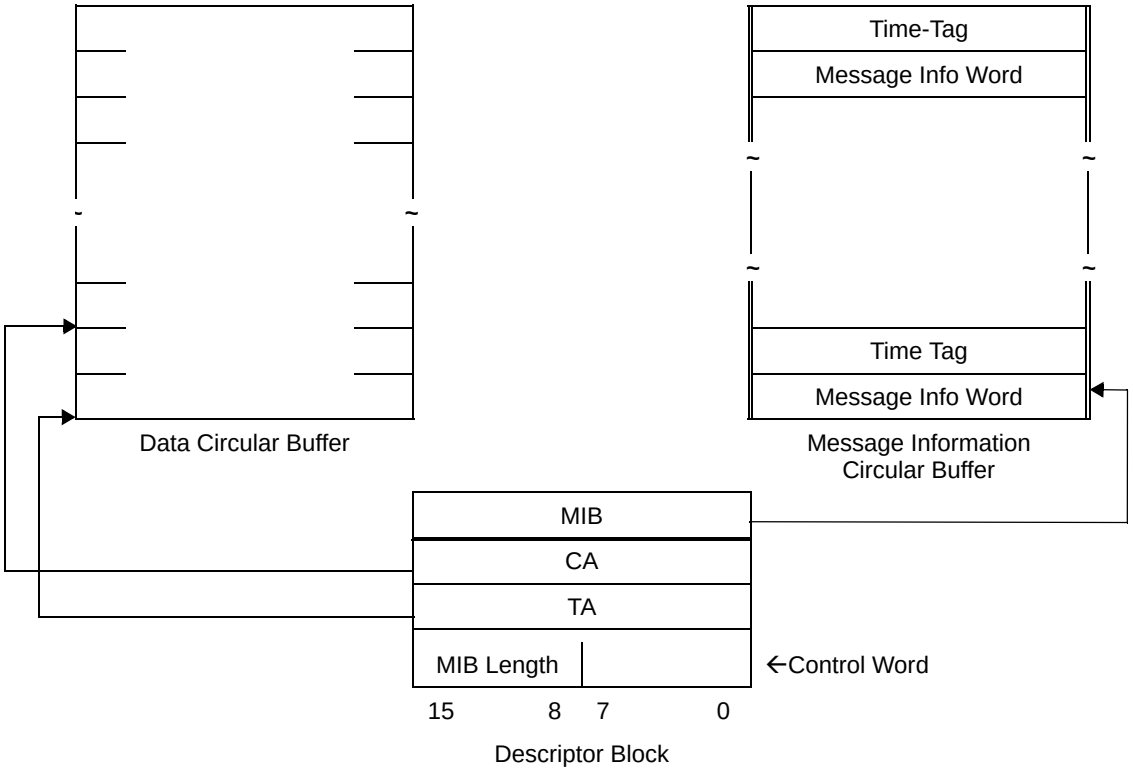


Figure 4-7 RT Mode #2 Descriptor Block

4.5 Mode Code and Subaddress

The *EXC-1553PCI/MCH* provides subaddress and mode code decoding that meets MIL-STD-1553B requirements. In addition, the channel has automatic internal illegal Command decoding for reserved. MIL-STD-1553B mode codes. Table 4-4 shows the channel's response to all possible mode code combinations.

T/R	Mode Code	Function	Operation
0	00000 – 01111	Undefined (w/o data)	1. Command Word stored 2. Status Word transmitted
0	10000	Undefined (with data)	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10001	Synchronize (with data)	1. Command Word stored 2. Data Word stored 3. Time-Tag counter loaded with Data Word value 4. Status Word transmitted
0	10010	Undefined	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10011	Undefined	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10100	Selected Transmitter Shutdown	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10101	Override Selected Transmitted Shutdown	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
0	10110 – 11111	Reserved	1. Command Word stored 2. Data Word stored 3. Status Word transmitted
1	00000	Dynamic Bus Control	1. Command Word stored 2. Dynamic Bus Acceptance bit set in outgoing Status Word if enabled in the Control Register 3. Status Word transmitted
1	00001	Synchronize	1. Command Word stored 2. Time Tag counter reset to 0000 (H) 3. Status Word transmitted

Table 4-4 Mode Code Description

T/R	Mode Code	Function	Operation
1	00010	Transmit Status Word	1. Command Word stored 2. Last Status Word 3. Status Word cleared after reset **Note**: The channel updates Status Word if illegalized.
1	00011	Initiate Self-Test	1. Command Word stored 2. Status Word transmitted 3. BIT initiated 4. TF bit set if BITF bit asserted
1	00100	Transmitter Shutdown	1. Command Word stored 2. Status Word transmitted 3. Alternate bus disabled
1	00101	Override Transmitter Shutdown	1. Command Word stored 2. Status Word transmitted 3. Alternate bus enabled **Note**: Reception of the override transmitter shut-down mode code does not enable a channel not previously enabled in the Control Register. Reset remote terminal mode code clears the transmitter shutdown function.
1	00110	Inhibit Terminal Flag Bit	1. Command Word stored 2. Terminal flag bit set to 0 and assertion disabled 3. Status Word transmitted
1	001111	Override Inhibit Terminal Flag	1. Command Word stored 2. Terminal flag bit enabled for assertion 3. Status Word transmitted
1	01000	Reset Remote Terminal	1. Command Word stored 2. Status Word transmitted 3. Software reset
1	01001 – 0 1111	Reserved	1. Command Word stored 2. Status Word transmitted
1	10000	Transmit Vector Word	1. Command Word stored 2. Service request bit set to a logic zero in out going Status 3. Status Word transmitted 4. Data Word transmitted 5. Clears the SRQ bit in the 1553 Status Word Bits Register
1	10001	Reserved	1. Command Word stored 2. Status Word transmitted 3. Data Word stored

Table 4-4 Mode Code Description (Continued)

T/R	Mode Code	Function	Operation
1	10010	Transmit Last Command	1. Command Word stored 2. Last Status Word transmitted 3. Last Command Word transmitted 4. Data Word stored (Transmit Last Command 5. Transmitted Data Word is all 0 after reset **Note**: The channel stores the Transmit Last Command mode code if illegalized and updates Status Word.
1	10011	Transmit BIT Word	1. Command Word stored 2. Status Word transmitted 3. BIT Word transmitted from BIT Word Register 4. Data Word stored (Transmit BIT Word)
1	10100 – 10101	Undefined (with data)	1. Command Word stored 2. Status Word transmitted 3. Data Word transmitted
1	10110 - 11111	Reserved	1. Command Word stored 2. Status Word transmitted 3. Data Word transmitted

Table 4-4 Mode Code Description (Continued)

.

4.6 Encoder and Decoder

The *EXC-1553PCI/MCH* receives the Command Word from the MIL-STD-1553 bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the Command is a receive Command, the channel processes each incoming Data Word for correct format, Word count, and contiguous data. If a message error is detected, the channel stops processing the remainder (if any) of the message, suppresses Status Word transmission, and asserts bit 09 (ME bit) of the Status Word.

The channel automatically compares the transmitted Word (encoder Word) with the reflected decoder Word by way of the continuous loopback feature. If the encoder Word and reflected Word do not match, the WRAPF bit is asserted in the BIT Word Register and an interrupt will be generated, if enabled. In addition to the loopback compare test, a timer precludes a transmission greater than 800ìsec. by the assertion of Fail-Safe Timer. This timer is reset upon receipt of another Command.

Remote Terminal Response-Time:

MIL-STD-1553A = 7 μsec.
MIL-STD-1553B = 10 μsec.
Data Contiguity Time-Out = 1.0 msec.

4.7 RT-to-RT Transfer Compare

The RT-to-RT Terminal Address compare logic ensures that the incoming Status Word's Terminal Address matches the Terminal Address of the transmitting RT specified in the Command Word. An incorrect match results in setting the message-error bit and suppressing transmission of the Status Word. (RT-to-RT transfer time-out = 55 to 59 μsec.). The channel does not check ME or SSYSF of the transmitting remote terminal when receiving.

4.8 Terminal Address

The *EXC-1553PCI/MCH* Terminal Address is programmed via the most significant six bits in the Operational Status Register: RTA[4-0] and RTPTY. The Terminal Address parity is odd; RTPTY is set to a logic state to satisfy this requirement. When the Operational Status Register bit 02 (TAPF) is set, this indicates incorrect Terminal Address parity. The Operational Status Register bit 02 is valid after the rising (final) edge of a reset.

For example:

RTA[4-0] = 05(H) = 00101
RTPTY = 1(H) = 1 Sum of 1s = 3 (odd), Operational Status Register Bit 02 = 0
RTA[4-0] = 04 (H) = 00100
RTPTY = 0 (H) = 0 Sum of 1s = 1 (odd), Operational Status Register Bit 02 = 0
RTA[4-0] = 04 (H) = 00100
RTPTY = 1 (H) = 0 Sum of 1s = 2 (even), Operational Status Register Bit 02 = 0

Note The channel checks the Terminal Address and parity after RT mode operation has been started. With Broadcast disabled, RTA(4:0) = 11111 operates as a normal RT address.

The BIT Word Register parity fail bit is valid after RT mode has been started.

The Terminal Address is also programmed via a write to the Operational Status Register. The channel loads the Terminal Address upon completion of the Control Register write that activates RT mode.

4.9 Reset

The software reset (see **Channel Reset Register,** page 2-11) is also equivalent to a hardware (power-on) reset and takes 5 μsec. to complete. Setting the Reset bit to 1 results in the immediate reset of the channel and termination of Command processing. The user is responsible for the re-initialization of the RT Mode for operation.

A Reset Remote Terminal mode code (Mode Code 01000, T/R = 1) clears the encoder/decoders, resets the Time Tag, enables the buses to the programmed host state, and re-enables the Terminal Flag for assertion. This reset is performed after the transmission of the 1553 Status Word.

4.10 MIL-STD-1553A/B Operation: RT Mode

To maximize flexibility, the *EXC-1553PCI/MCH* can operate in many different systems that use various protocols. Specifically, two of the protocols that the channel may be used with are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, configure the channel through the Control register (XMTSW Bit 00) and the Operational Status register (A/B_STD Bit 07).

Table 4-5 defines the three ways to program the channel.

A/B STD	XMTSW	RESULT (protocol selected)
0	X	1553B response, 1553B Standard
1	0	1553A response, 1553A Standard
1	1	1553A response, auto execute the TRANSMIT STATUS WORD mode code.

Table 4-5 MIL-STD-1553A/B Operation: RT Mode

When configured as a remote terminal to meet MIL-STD-1553A, the *EXC-1553PCI/MCH* will operate as follows:

- Responds with a Status Word within 7μsec.
- Ignores the T/R bit for all mode codes.
- All mode codes are defined without data.
- All mode codes use mode code transmit control and information Words.
- Mode code 00000 is defined as dynamic bus control (DBC).
- Subaddress 00000 defines a mode code.
- ME and TF bits are defined in the 1553 Status Word; all other Status Word bits are programmable (i.e., NO BUSY mode, etc.)
- Broadcast of all mode codes, except Mode Code 00000 (DBC) and mode code 00010 (transmit Status Word if enabled), is allowed.
- To illegalize a Mode Code, the user needs to illegalize both the receive and transmit versions.
- Illegalization of row 1F (H) is not automatic.

5 Bus Monitor Operation

Chapter 5 describes *EXC-1553PCI/MCH* operation in Bus Monitor (BM) mode. The topics covered are:

5.1 Bus Monitor Message Processing 5-2
5.1.1 Error Condition Message Processing 5-2
5.1 Control Registers: BM Mode 5-3
5.1.1 Control Register 5-4
5.1.2 Operational Status Register 5-5
5.1.3 Current Command Register 5-6
5.1.4 Interrupt Mask Register 5-6
5.1.5 Pending Interrupt Register 5-7
5.1.6 Interrupt Log List Pointer Register 5-7
5.1.7 BIT Word Register 5-8
5.1.8 Time Tag Register 5-8
5.1.9 Initial Monitor Block Pointer Register 5-9
5.1.10 Initial Monitor Data Pointer Register 5-9
5.1.11 Monitor Block Counter Register 5-9
5.1.12 Monitor Filter Hi Register 5-10
5.1.13 Monitor Filter Lo Register 5-10
5.1 Bus Monitor Architecture 5-11
5.1.1 Message Information Word 5-11
5.1.2 Command Words 5-12
5.1.3 Data Pointer 5-12
5.1.4 Status Words 5-13
5.1.5 Time Tag 5-13
5.1.6 Reserved 5-13
5.1 Bus Monitor Block Chaining 5-13
5.1 Memory Architecture 5-14
5.1 RT/Concurrent Monitor Operation 5-15
5.1 MIL-STD-1553A/B Operation: BM Mode 5-16

5.1 Bus Monitor Message Processing

To process messages, the *EXC-1553PCI/MCH* uses data supplied in the Control Registers along with RAM memory. There are eight 16-bit memory locations for each message called a monitor block, seven are used and one is reserved. The monitor block is updated at the end of command processing. The following paragraphs discuss the command block in detail.

The user allocates memory spaces for each monitor block. The top of the monitor blocks can reside at any address location. The Control Registers are initialized by the host and linked to the Monitor Block via the Initial Monitor Block Pointer Register and the Monitor Block Counter Register contents. Each monitor block contains a Message Information Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, and Time Tag. For a full description of each location, see section "Bus Monitor Architecture" on page 11.

The Message Information Word allows the channel to inform the user on which bus the command was received, whether the message was an RT-to-RT transfer, and conditions associated with the message. The channel also stores each Command Word associated with the message in the appropriate location. For normal 1553 commands, only the first Command Word location will contain data. For RT-to-RT commands, the second Command Word location will contain data, and bit 08 in the Message Information Word will be set.

For each command, the Data Pointer is read to determine where to store data words. The channel stores data sequentially from the top memory location. The channel also stores each status word associated with the message in the appropriate location. For normal 1553 commands, only the first status word location will contain data. For RT-to-RT commands, the second status word location will contain data.

The channel begins monitoring after Control Register bit 15 = 1 (i.e., Setting TERACT and STEX bits to 1). After reception, the channel begins post-processing. Command post-processing involves storing data to memory. An optional interrupt log entry is performed after a monitor is entered. Monitor Time-Out:

- MIL-STD-1553A = 9 μsec.
- MIL-STD-1553B = 15 μsec.

5.1.1 Error Condition Message Processing

When the monitor detects as error condition, either, in the Command Word, Data Words, or the RT's status, the monitor block will not store the data. The monitor block counter increments. The initial message Data Pointer remains constant. The monitor block pointer increments. Message information bits of the monitor block are changed to reflect the error. An interrupt is given indicating a message has occurred.

See **Message Information Bits**, page page 12.

5.1 Control Registers: BM Mode

The control registers are read/write unless otherwise stated. All control registers **must** be accessed in word mode. All Control Register bits are active high and are reset to 0 unless otherwise stated.

Figure **5-1** illustrates the control registers for Bus Monitor mode.

Reserved	0020-003E H
Monitor Filter Register Lo	001E H
Monitor Filter Register Hi	001C H
Monitor Block Counter Register	001A H
Initial Monitor Data Pointer Register	0018 H
Initial Monitor Command Block Pointer Register	0016 H
Reserved	0010-0014 H
Time Tag Register	000E H
BIT Word Register	000C H
Interrupt Log List Pointer Register	000A H
Pending Interrupt Register	0008 H
Interrupt Mask Register	0006 H
Current Command Block Register	0004 H
Operational Status Register	0002 H
Control Register	0000 H

Figure 5-1 Control Registers Map: BM Mode

5.1.1 Control Register

Address: 0000 (H)
Read/Write

Use the Control Register to configure the channel for BM operation. To make changes to the BM and to this register, the STEX bit (bit 15) must be logic 0.

Note: The user has 5 μsec. after the TERACT bit (bit 00 of the Operational Status Register) is active, to stop operation.

Bit	Bit Name	Description
15	**STEX**	Start Execution 1 = Initiates channel operation 0 = Inhibits channel operation After execution begins, writing a logic 0 will halt the channel after completing the current 1553 message.
14	**SBIT**	Start BIT 1 = Places the channel into the Built-In Test routine. The BIT test takes 1 msec. to execute and has a fault coverage of 93.4%. Once the channel has been started, the host must halt the channel in order to place it into the Built-In Test mode (STEX = 0). **Note:** If Start BIT (SBIT) and Start Execution (STEX) are both set on one register write, BIT has priority.
11-13	**Reserved**	Set to 0
10	**ETCE**	External Timer Clock Enable 1 = Enables an external clock used with an internal counter for variable minor frame timing **Note:** The user can only change the clock frequency before starting the device (i.e. setting bit 15 of register 0 to a login 1.
09	**ERTO**	Extended Response Time-Out 1 = Enables the extended response time-out option and forces the BM Mode to look for an RTs response time in 30 μsec. or generate time-out errors. 0 = Enables for the standard time-out in 14 μsec.
06-08	**Reserved**	Set to 0
05	**BMTC**	Bus Monitor Control. This bit determines whether the channel will monitor all RTs or selected RTs. 1 = The channel will monitor only the RTs as specified in the Monitor Filter Hi and Lo registers. 0 = The channel will monitor all RTs.
04	**BCEN**	Broadcast Enable 1 = Enables RT #31 to be used as a message broadcast 0 = Enables RT #31 as a normal address.
02-03	**Reserved**	Set to 0
01	**INTEN**	Interrupt Log List Enable. 1 = Enables the interrupt log list. 0 = Prevents the logging of interrupts as they occur.
00	**Reserved**	Set to 0

5.1.2 Operational Status Register

Address: 0002 (H) Read/Write

The Operational Status Register reflects pertinent status information for the channel and is not reset to 0000 (H) on reset. Instead, the bit A/B_STD is set to 1.

Note: To make changes to the Monitor and this register, the STEX bit (Bit 15 in the Control Register) must be logic 0.

Bit	Bit Name	Description
10-15	**Reserved**	Set to 0
09	**MSEL1**	Mode Select 1. In conjunction with Mode Select 0, this bit determines the channel's mode of operation.
08	**MSEL0**	Mode Select 0. In conjunction with Mode Select 1, this bit determines the channel's mode of operation.

MSEL1	MSEL0	Mode of Operation
0	0	BC
0	1	RT
1	0	BM
1	1	RT/ Concurrent BM Mode

07	**A/B_STD**	Military Standard 1553A or 1553B. This bit determines if the channel will operate under MIL-STD-1553A or 1553B protocol. 1 = Forces the channel to declare a time-out error condition if the RT9 has not responded in 9 μsec. 0 = Allows the channel to declare a time-out error condition if the RT has not responded in 15 μsec.
04-06	**Reserved**	These read-only bits are not applicable.
03	**EX**	Channel Executing. This read-only bit indicates whether the channel is presently executing or is idle. 1 = The channel is executing. 0 = The channel is idle.
02	**Reserved**	This read-only bit is not applicable.
01	**Ready**	Channel-Ready. This read-only bit is cleared on reset. 1 = The channel has completed initialization or BIT, and regular operation may begin.
00	**TERACT**	Channel Terminal Active. This read-only bit is cleared on reset. 1 = The channel is presently processing a 1553 message.

5.1.3 Current Command Register

Address: 0004 (H)
Read only

The Current Command register contains the last valid command that was transmitted over the 1553 bus. In an RT-to-RT transfer, this register will update as each of the two commands are received by the Bus Monitor.

Bit	Bit Name	Description
00-15	**CC[15-0]**	Current Command. These bits contain the latest 1553 command that was transmitted by the Bus Monitor.

5.1.4 Interrupt Mask Register

Address: 0006 (H)
Read/Write

The *EXC-1553PCI/MCH* interrupt architecture allows the host to mask or temporarily disable the service of interrupts. While masked, interrupt activity does not occur. The unmasking of an interrupt after the event occurs does not generate an interrupt for that event. An interrupt is masked only if the corresponding bit of this register is set to a logic 0.

Bit	Bit Name	Description
12-15	**Reserved**	Set to 0
11	**MERR**	Message Error Interrupt
01-10	**Reserved**	Set to 0
00	**MBC**	Monitor Block Counter Interrupt

5.1.5 Pending Interrupt Register

Address: 0008 (H)
Read only

The Pending Interrupt register is used to identify which of the interrupts occurred during operation. All register bits are cleared on a host read.

Bit	Bit Name	Description
12-15	**Reserved**	Ignore on read.
11	**MERR**	Message Error Interrupt 1 = A message error occurred. The channel can detect Manchester, sync-field, word count, 1553 word parity, bit count, and protocol errors. This bit will be set and an interrupt generated (if not masked) after message processing is complete.
01-10	**Reserved**	Ignore on read.
00	**MBC**	Monitor Block Counter Interrupt This bit is set if the channel's monitor block counter reaches 0 (transition from 1 to 0) **Note:** The monitor does not discriminate between error-free messages and those messages with errors

5.1.6 Interrupt Log List Pointer Register

Address: 000A (H)
Read/Write

The Interrupt Log List Pointer indicates the starting address of the Interrupt Log List. The Interrupt Log List is a 32-word ring-buffer that contains information pertinent to the service of interrupts.

The *EXC-1553PCI/MCH* architecture requires the location of the Interrupt Log List on a 32-word boundary. The most significant 11 bits of this register designate the location of the Interrupt Log List within a 64K-word memory space. Initialize the lower 5 bits of this register to a logic 0 by the host. The channel controls the lower 5 bits to implement the ring-buffer architecture. Read this register to determine the location and number of interrupts within the Interrupt Log List (least significant 5 bits).

Bit	Bit Name	Description
00-15	**ILLP[15-0]**	Interrupt Log List Pointer Bits. **Note:** Bits 05-15 indicate the starting Base address while bits 00-04 indicate the ring location of the Interrupt Log List.

5.1.7 BIT Word Register

Address: 000C (H)
Read/Write

The BIT Word Register contains information on the current status of the channel hardware. The user defines the lower 8 bits of this register.

Bit	Bit Name	Description
15	**DMAF**	DMA Fail. 1 = All the channel's internal DMA activity was not completed within 7 μsec.
13-14	**Reserved**	Ignore on read
12	**BITF**	BIT Fail. 1 = A BIT failure. Interrogate bits 11and 10 to determine the specific bus that failed.
11	**BUAF**	Bus A Fail. 1 = A BIT test failure in Bus A.
10	**BUBF**	Bus B Fail. 1 = A BIT test failure in Bus B.
09	**MSBF**	Memory Test Fail. Most significant memory byte failure.
08	**LSBF**	Memory Test Fail. Least significant memory byte failure.
00-07	**UDB[7-0]**	User-Defined Bits.

5.1.8 Time Tag Register

Address: 000E (H)
Read only

The Time Tag register reflects the state of a 16-bit free running ring counter in the RT and Bus Monitor modes. This counter will remain a free running counter as long as the channel is not in a reset mode. The resolution of this counter is 64 μsec/bit. The Time Tag counter begins operation on the falling (final) edge of the reset pulse.

Bit	Bit Name	Description
00-15	**TT[15-0]**	Time Tag Counter Bits. These bits indicate the state of the 16-bit internal counter.

5.1.9 Initial Monitor Block Pointer Register

Address: 0016 (H)
Read/Write

The Initial Monitor Block Pointer register contains the starting location of the Monitor Blocks.

Note: Do not change this register while BM mode is active (i.e., Operational Status Register, bit 03 = 1).

Bit	Bit Name	Description
00-15	**MBA[15-0]**	Initial Monitor Block Address. These bits indicate the starting location of the Monitor Block.

5.1.10 Initial Monitor Data Pointer Register

Address: 0018 (H)
Read/Write

The Initial Monitor Data Pointer register contains the starting location of the Monitor Data.

Note: Do not change this register while BM mode is active (i.e., Operational Status Register, bit 03 = 1).

Bit	Bit Name	Description
00-15	**MBA[15-0]**	Initial Monitor Data Address. These bits indicate the starting location of the Monitor Data.

5.1.11 Monitor Block Counter Register

Address: 001A (H)
Read/Write

The Monitor Block Counter register contains the number of Monitor Blocks the user wants to log. After execution begins, the register automatically decrements as commands are logged. When the register is decremented from 1 to 0, an interrupt will be generated, if enabled. The channel will start over at the initial pointers as identified in the Initial Monitor Block Pointer Register and the Initial Monitor Data Pointer Register.

Note: It is recommended that this register not be changed while the BM mode is active (i.e., Operational Status Register, bit 03 = 1).

Bit	Bit Name	Description
00-15	**MBC[15-0]**	Monitor Block Count. These bits indicate the number of Monitor Blocks to log.

5.1.12 Monitor Filter Hi Register

Address: 001C (H)
Read/Write

The Monitor Filter Hi Register determines which RTs (RT 31 through RT 16) the channel will monitor.

Bit	Bit Name	Description
00-15	**MFH[31-16]**	Monitor Filter. These bits determine which RT to monitor.

5.1.13 Monitor Filter Lo Register

Address: 001E (H)
Read/Write

The Monitor Filter Lo Register determines which RTs (RT 15 through RT 0) the channel will monitor.

Bit	Bit Name	Description
00-15	**MFL[15-00]**	Monitor Filter. These bits determine which RT to monitor.

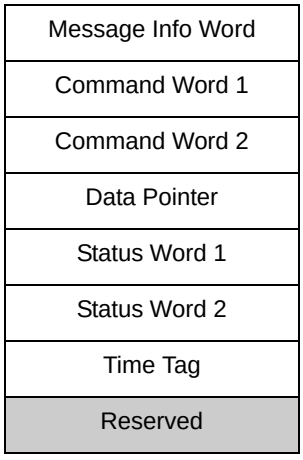
5.1 Bus Monitor Architecture

To meet the MIL-STD-1553 monitor requirements, the channel uses a Monitor Block architecture that takes advantage of both Control Registers and RAM. The Monitor Block, that is located in contiguous memory, requires eight 16-bit locations for each message.

These eight locations include:

- A Message Information Word
- Two Command Word locations
- A Data Pointer
- Two Status Word locations
- A Time-Tag location
- A reserved location

The user must initialize the starting locations of the Monitor Block, the Data Pointer, the Block Counter, and the Interrupt Log Pointer. From then on, the channel will build a Monitor Block for each message it receives over the 1553 bus. Figure 5-2 shows a diagram of the Monitor Block followed by a description of each location associated with the Monitor Block.



5.1.1 Message Information Word

The first memory location of each Monitor Block contains the message information word. Each information word contains the opcode, retry number, bus definition, RT-to-RT messages, and the message information.

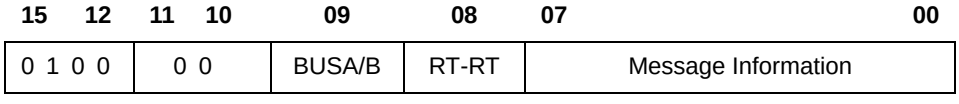


Figure 5-2 Message Information Word

Bit Number	Description
12-15	Default. With the Monitor Block architecture resembling the BC Command Block architecture, these bits default to a 0100 state (which is the Execute and Continue opcode) in case the monitor must switch to the BC mode of operation.
10-11	Default. With the Monitor Block architecture resembling the BC, these bits default to a '00' state. If the monitor must switch to the BC, the retries will be set at four per message.
09	Bus A/B. This bit defines on which of the two buses the command was received. (Logic 1 = Bus A, Logic 0 = Bus B).
08	RT-to-RT Transfer. This bit defines whether or not the message associated with this Monitor Block was an RT-to-RT transfer and whether the channel saved the second command word. This bit will be set only if the channel is instructed to monitor the Receive RT.
00-07	**Message Information Bits.** These bits define the conditions of the message received by the channel for that particular Monitor Block. In an RT-to-RT transfer, the information applies to the complete message:
07	Message Error. This bit will be set if the monitor detects an error in either the Command Word, Data Words, or the RT's status.
06	Mode Code without Data. This bit will be set if the monitor detects that the command being processed is a mode code without data words.
05	Broadcast. This bit will be set if the monitor detects that the command being processed, is a broadcast message.
04	Reserved
03	Time-Out Error. This bit will be set if the RT did not receive the proper number of Data Words, e.g., the number of Data Words received was less than the word count specified in the Command Word.
02	Overrun Error. This bit will be set if the RT received a word when none were expected or the number of Data Words received was greater than expected.
01	Parity Error. This bit will be set if a parity error has occurred on the Data Words or the RT's status word.
00	Manchester Error. This bit will be set if a Manchester error has occurred on either the Data Words or the RT's status word.

5.1.2 Command Words

The next two locations in the channel Monitor Block are for Command Words. In non-RT-to-RT 1553 messages, only the first Command Word will be stored. However, in an RT-to-RT transfer, the first command word is the Receive Command and the second Command Word is the Transmit Command.

5.1.3 Data Pointer

The fourth location in the Monitor Block is the Data Pointer. This pointer points to the first memory location to store the Data Words associated with the message for this block. The data associated with each individual message will be stored contiguously. This data structure allows the channel to store the specified number of data words.

Note: In an RT-to-RT transfer, the BM uses the Data Pointer as the location in memory to store the transmitting data in the transfer.

5.1.4 Status Words

The next two locations in the Monitor Block are for Status Words. As the RT responds to the BC's command, the corresponding Status Word will be stored in Status Word 1. However, in an RT-to-RT transfer, the first status word will be the status of the Transmitting RT while the second Status Word will be the status of the Receiving RT.

5.1.5 Time Tag

The seventh location in the Monitor Block is the Time Tag associated with the message. The Time Tag is stored into this location at the end of message processing (i.e., captured after the command is validated).

5.1.6 Reserved

The last location in the Monitor Block is reserved.

5.1 Bus Monitor Block Chaining

The host determines the first Monitor Block by setting the start address in the Initial Monitor Block Pointer Register. Figure **5-3** shows the Monitor Block as the blocks execute in a contiguous fashion.

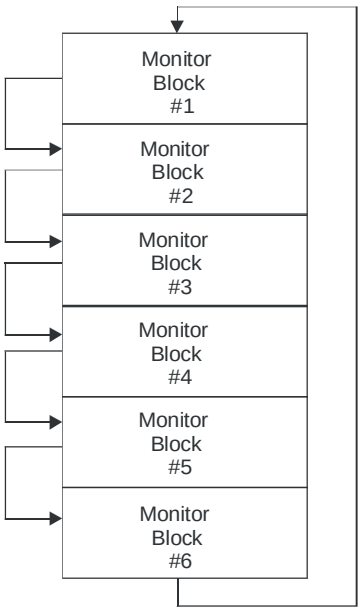


Figure 5-3 Bus Monitor Block Structuring

5.1 Memory Architecture

The configuration shows the Monitor Blocks, data locations and the Interrupt Log List as separate entities. Figure **5-4** shows that the first block of memory is allocated for the Monitor Blocks. Notice that the Initial Monitor Block Pointer Register points to the initial Monitor Block location, the Initial Monitor Data Pointer Register points to the initial Data location, Interrupt Log List Pointer Register points to the Interrupt Log, and the Monitor Block Counter Register contains the Monitor Block count. After execution begins, the channel will build command blocks and store Data Words until the count reaches 0. When the count reaches 0, the channel will simply wrap back to the initial values and start again.

Table 1:

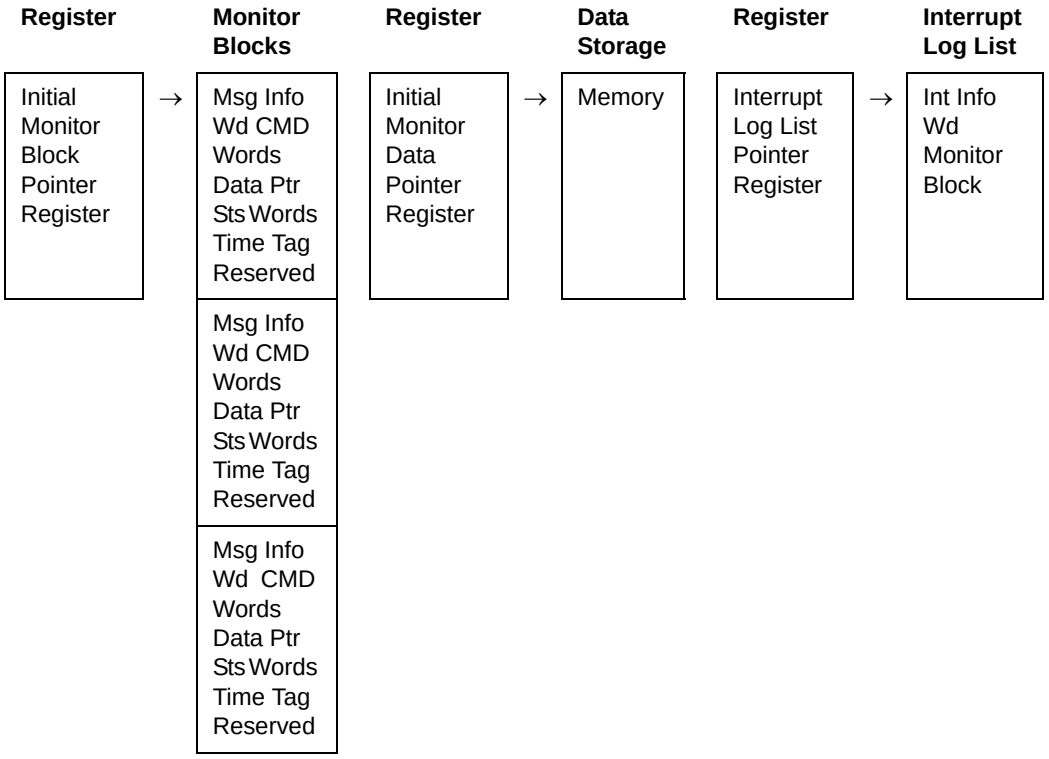


Figure 5-4 Memory Architecture for Bus Monitor Mode

5.1 RT/Concurrent Monitor Operation

For applications that require simultaneous Remote Terminal and Bus Monitor operation, the channel should be configured as both a Remote Terminal and Bus Monitor. This feature allows the RT to communicate on the bus for one specific address and to monitor the bus for other specific addresses. Configuration as both Bus Monitor and RT precludes the channel from monitoring its own Remote Terminal address.

When the channel is configured as both RT and Bus Monitor, the RT has priority over the Bus Monitor. For example, commands to the RT will always take priority over commands for the Bus Monitor. The examples below describe what happens if the RT is defined for terminal address 1 and the Bus Monitor is to monitor terminal address 12.

Example 1:

Bus A	CMD/TA = 12		
Bus B		CMD/TA = 1	

In this example, the Bus Monitor will decode the first command on bus A, realize the message is for terminal address 12, and start monitoring the message. However, as soon as the channel realizes the second command on bus B is to terminal address 1, the RT will take priority and begin RT message processing.

Example 2:

Bus A	CMD/TA = 1		
Bus B		CMD/TA = 12	

In Example 2, the RT will decode the first command on bus A, realize the message is for terminal address 1, and start message processing. As the message on bus B is received, the channel will realize it is to terminal address 12, but since the RT has priority, the Bus Monitor will not switch to the bus monitor mode.

The above examples also apply to an RT-to-RT message. For example, if the first command in an RT-to-RT transfer matches the terminal address of the RT, the entire message will be stored (Message 1). However, if the first command in an RT-to-RT transfer matches the terminal address of the Bus Monitor and the second command matches the terminal address of the RT, the RT will take priority and only the RT message is stored (Message 2).

Example 3:

Message 1	CMD/TA = 1	CMD/TA = 12

Message 2	CMD/TA = 12	CMD/TA = 1

This is an RT-to-RT message.

5.1 MIL-STD-1553A/B Operation: BM Mode

To maximize flexibility, the *EXC-1553PCI/MCH* can operate in many different systems that use various protocols. Specifically, two of the protocols that the channel may be used with are MIL-STD-1553A and MIL-STD-1553B. To meet these protocols, configure the channel through the Control register (ERTO Bit 09) and the Operational Status register (A/B_STD Bit 07).

Table **5-1** defines the four ways to program the *EXC-1553PCI/MCH*.

A/B_STD	ERTO	RESULT
0	0	1553B standard, 1553B response (in 14 μsec.)
0	1	1553B standard, extended response (in 30 μsec.)
1	0	1553A standard, 1553A response (in 9 μsec.)
1	1	1553A standard, extended response (in 21 μsec.)

Table 5-1 MIL-STD-1553A/B Operation: BC Mode

When configured as a MIL-STD-1553A bus controller, the *EXC-1553PCI/MCH* will operate as follows:

- Looks for the RT response within 9 μsec.
- Ignores the T/R bit for all mode codes
- Defines all mode codes without data
- Defines subaddress 00000 as a mode code

6 Channel Interrupt Architecture

Chapter 6 describes the channel interrupt architecture. The topics covered are:

6.1 Overview 6-1
6.1.1 Interrupt Identification Word (IIW) 6-2
6.1.2 Interrupt Address Word (IAW) 6-2
6.1.3 Interrupt Log List Address 6-3

6.1 Overview

The *EXC-1553PCI/MCH* interrupt architecture involves three Control Registers, an Interrupt Log List, and the interrupt line. The three Control Registers include a Pending Interrupt Register, Interrupt Mask Register, and Interrupt Log List Register. The Pending Interrupt Register contains information that identifies the events generating the interrupts. The Interrupt Mask Register allows the user to mask or disable the generation of interrupts. The Interrupt Log List Register contains the base address of a 32-word interrupt ring buffer.

The lower twelve interrupt bits of the Pending Interrupt Register are entered into the Interrupt Log List, if the Interrupt Log List is enabled.

The interrupt architecture allows for the entry of 16 interrupts into a 32-word ring buffer. The *EXC-1553PCI/MCH* automatically handles the interrupt logging overhead. Each interrupt generates two words of information to assist the host in performing interrupt processing. The Interrupt Identification Word (IIW) identifies the type(s) of interrupt that occurred. The Interrupt Address Word (IAW) identifies the interrupt source (e.g., subaddress or command block) via a 16-bit address.

6.1.1 Interrupt Identification Word (IIW)

The Interrupt Identification Word is a 16-bit word identifying the interrupt type. The format is similar to the Pending Interrupt Register. The host reads the IIW to determine which interrupt event occurred. The bit description for the IIW is:

Bit	Bit Name	Description
12-15	Reserved	Set to 0
11	MERR	Message Error Interrupt (All modes)
10	SUBAD	Subaddress Accessed Interrupt (RT Mode)
09	BDRCV	Broadcast Command Received Interrupt (RT Mode)
08	IXEQ0	Index Equal Zero Interrupt (RT Mode)
07	ILCMD	Illegal Command Interrupt (RT Mode)
06	Reserved	Set to 0
05	EOL	End Of List (BC Mode)
04	ILLCMD	Illogical Command (BC Mode)
03	ILLOP	Illogical Opcode (BC Mode)
02	RTF	Retry Fail (BC Mode)
01	CBA	Command Block Accessed (BC Mode)
00	MBC	Monitor Block Count Equal Zero (BM Mode)

Interrupt Identification Word (IIW)

6.1.2 Interrupt Address Word (IAW)

The Interrupt Address Word is a 16-bit word that identifies the interrupt source. Depending on the mode of operation (i.e., RT, BC, or BM), the IAW has different meanings. In the RT mode operation, the IAW identifies the subaddress or mode code descriptor that generated the interrupt. For the BC mode of operation, the IAW points to the command block addressed when the interrupt occurred. In the BM mode of operation, the IAW marks the monitor counter count when the interrupt occurred. Use the IAW with the Initial Monitor Command Block Pointer Register to determine the monitor command block that generates the interrupt.

When in RT/Concurrent-BM mode, the user determines if the IAW contains information for the RT or the BM. The determination is made by comparing the contents of the IAW base address with the descriptor base address. If a match occurs, then the IAW contains a subaddress or mode code identifier. If no match occurs, the IAW contains monitor counter information.

6.1.3 Interrupt Log List Address

The Interrupt Log List resides in a 32-word ring buffer. The host defines the location buffer, within the memory space, via the Interrupt Log List Register. Restrict the ring buffer address to a 32-word boundary.

During initialization write a value to the Interrupt Log List Pointer Register. Initialize the least significant five bits to a logic 0. The most significant 11 bits determine the base address of the buffer. The channel increments the ring buffer pointer on the occurrence of the first interrupt, storing the IIW and IAW at buffer locations 00 (H) and 02 (H) respectively. The channel logs ensuing interrupts sequentially into the ring buffer until interrupt number 16 occurs. The channel enters interrupt 16's IIW in buffer location 3C (H) and the IAW at location 3E (H).

The channel increments the ring buffer pointer as interrupts occur. The least significant five bits of the Interrupt Log List Pointer register reflect the ring buffer pointer value. Table 6-1 shows the ring buffer architecture.

The user reads the ring buffer pointer value to determine the number of interrupts that have occurred. By extracting, the least significant five bits from the Interrupt Log List Register, and logical shifting the data once to the right, the host determines the number of interrupt events.

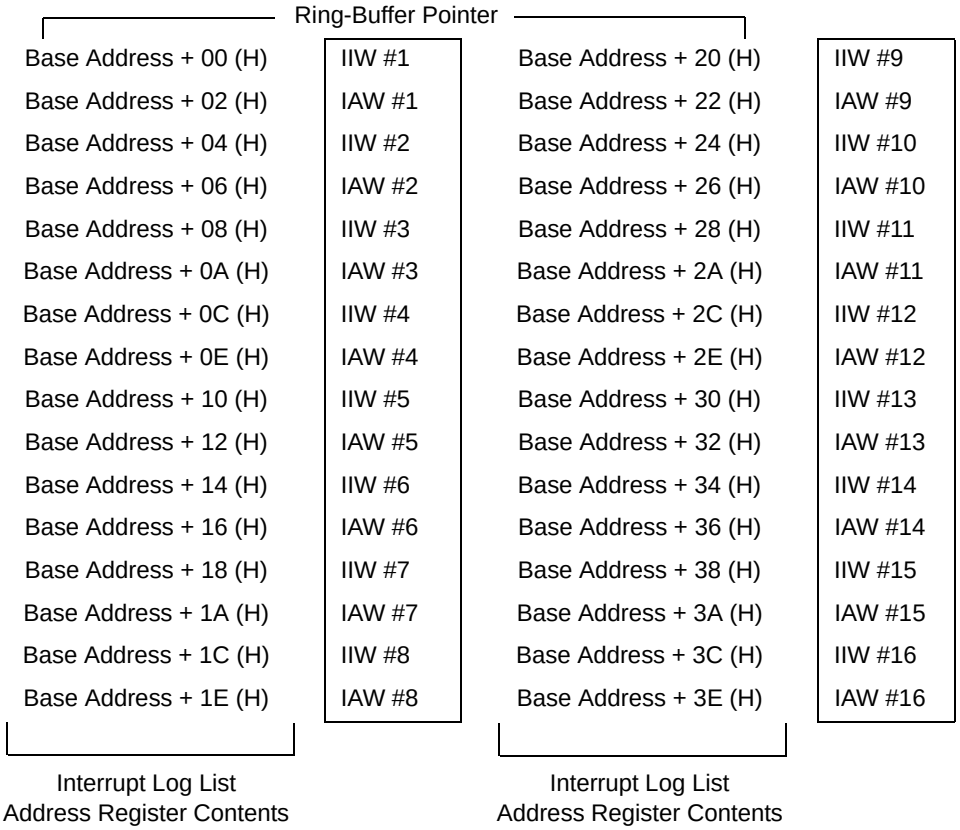


Table 6-1 Interrupt Ring Buffer

7 Mechanical And Electrical Specifications

Chapter 7 describes the mechanical and electrical specifications of the *EXC-1553PCI/MCH*. The topics discussed are:

7.1 Board Layout 7-2
7.1.1 *EXC-1553PCI/MCH* Board Layout 7-2
7.1.2 EXC-1553cPCI/MCH Board Layout 7-3
7.2 LED Indicators 7-4
7.2.1 *EXC-1553PCI/MCH* LED Indicators 7-4
7.2.2 EXC-1553cPCI/MCH LED Indicators 7-4
7.3 DIP Switches 7-4
7.3.1 Selected ID DIP Switch [SW1] 7-4
7.3.2 Multiple Board Applications 7-5
7.4 Jumpers 7-6
7.4.1 Channel 0 – Channel 3 1553 Coupling Mode Select Jumpers [JP2–JP17] 7-6
7.4.2 Factory Default Jumper Settings 7-6
7.5 Connectors 7-7
7.5.1 Connector J1 Pinouts 7-8
7.5.2 Communication I/O Signals Description of Connector J1 7-9
7.5.3 PCI Bus Edge Connector Pinouts 7-11
7.5.4 cPCI Bus Connector Pinouts 7-12
7.6 Power Requirements 7-12

7.1 Board Layout

7.1.1 *EXC-1553PCI/MCH* Board Layout

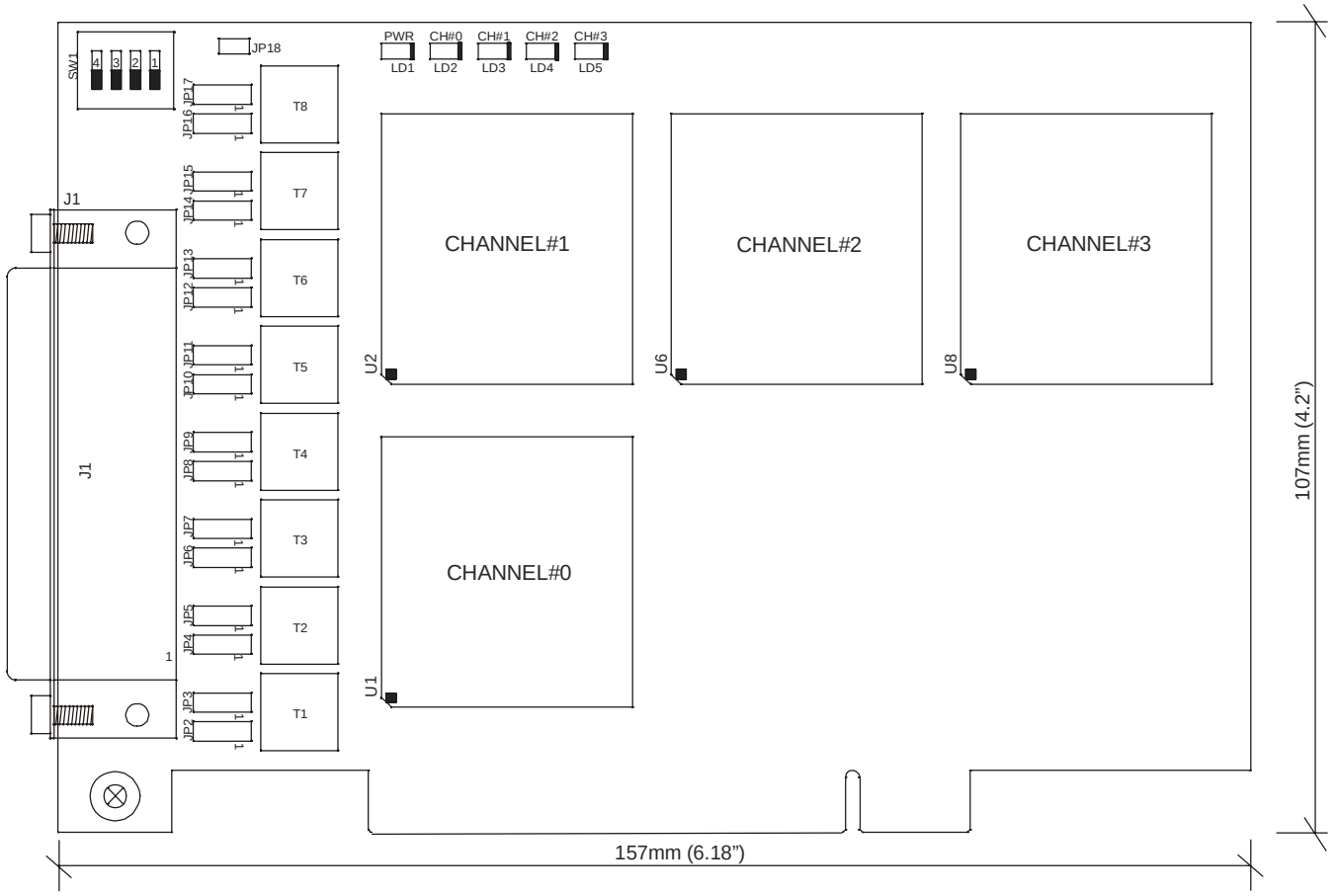


Figure 7-1 *EXC-1553PCI/MCH* Board Layout

7.1.2 EXC-1553cPCI/MCH Board Layout

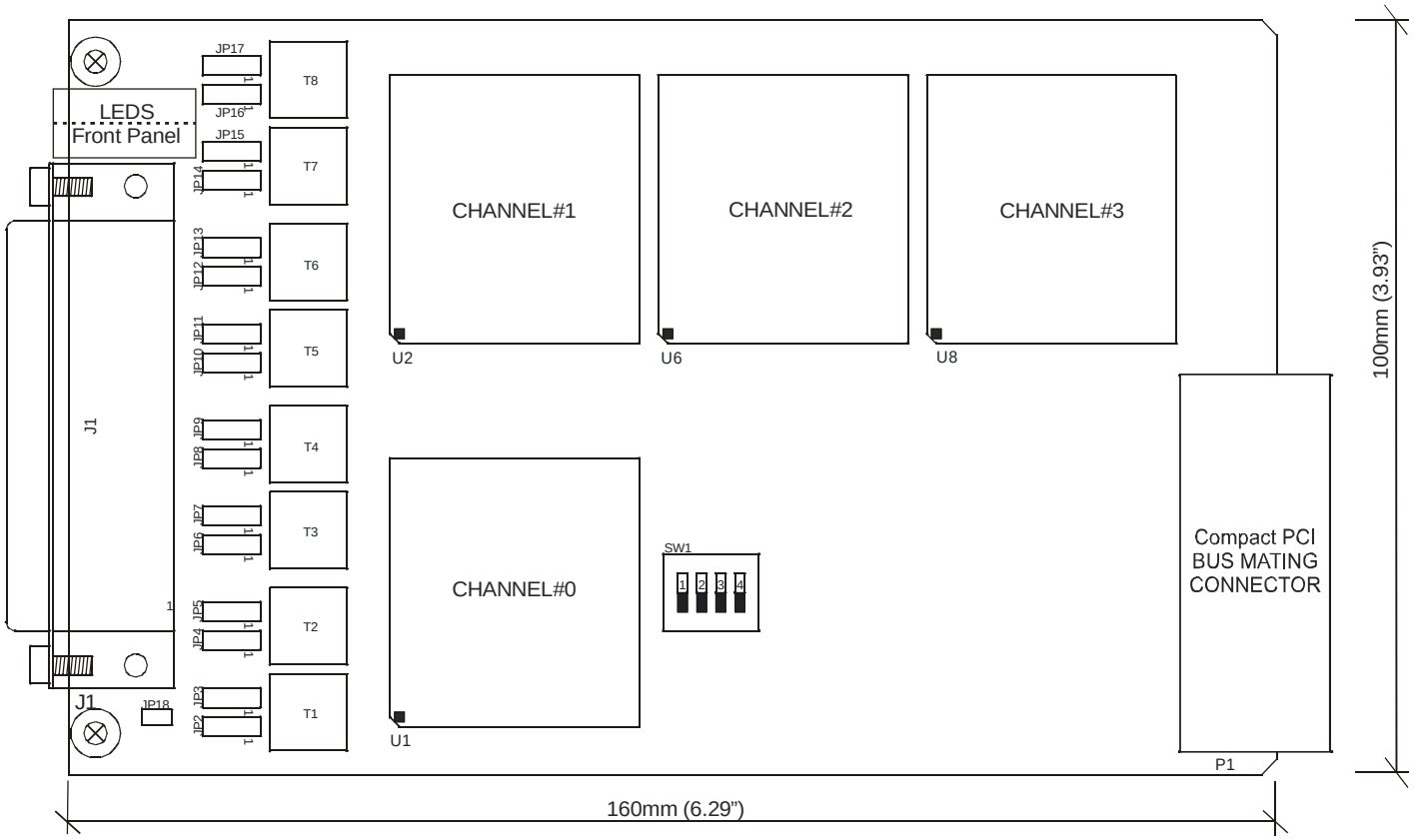


Figure 7-2 EXC-1553cPCI/MCH Board Layout

7.2 LED Indicators

7.2.1 *EXC-1553PCI/MCH* LED Indicators

The *EXC-1553PCI/MCH* contains five LEDs:

LED	Name	Indication
LD1	PWR	Power is being supplied to the board
LD2.	CH#0	A message is being processed by channel 0
LD3	CH#1	A message is being processed by channel 1
LD4	CH#2	A message is being processed by channel 2
LD5	CH#3	A message is being processed by channel 3

***EXC-1553PCI/MCH* LED Indicators**

7.2.2 EXC-1553cPCI/MCH LED Indicators

The *EXC-1553cPCI/MCH* contains four LEDs on the **front panel**. Each Led indicates that a message is being processed by that specific channel.

LED	Name	Indication
LD1.	CH#0	A message is being processed by channel 0
LD2	CH#1	A message is being processed by channel 1
LD3	CH#2	A message is being processed by channel 2
LD4	CH#3	A message is being processed by channel 3

EXC-1553cPCI/MCH LED Indicators

7.3 DIP Switches

The *EXC-1553PCI/MCH* contains one DIP switch (SW1).

7.3.1 Selected ID DIP Switch [SW1]

This four contact DIP switch provides the board's 'Select ID'. It represents a four bit number of which position #1 is the most significant bit. When a specific bit of the switch is:

- **open** or **off** a value of "1" will be set for that bit
- **closed** or **on** a value of "0" will be set for that bit

7.3.2 Multiple Board Applications

To provide a unique 'Selected ID', to identify a board by the application software in a multiple board application, the DIP switch should be set differently for each board. For example:

Board	ID#1	ID#3
Bit 1	closed/on	closed/on
Bit 2	closed/on	closed/on
Bit 3	closed/on	open/off
Bit 4	open/off	open/off

Dip Switch settings for unique 'Selected ID'

For multiple board applications, each board's device number may be set by using the Excalibur configuration utility program provided with the drivers, and by setting the 'unique ID' to match that set on the DIP switch shown in Figure 7-3.

Select ID	1	2	3	4
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1

Note: Bits 1 and 2 are not used and should be kept closed

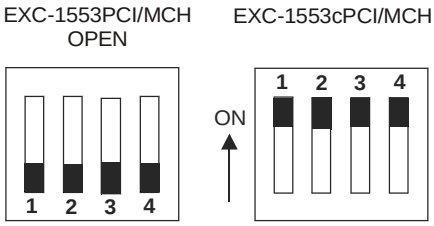


Figure 7-3 DIP Switch SW1 with all switches set to closed /on (Select ID#0)

7.4 Jumpers

Jumper Headers are provided on the board. The headers are mounted with 2 mm shorting blocks according to the default board setup. (See section **7.4.2 Factory Default Jumper Settings**, on page 7-6.) In high vibration environments these jumpers can be soldered or "wire-wrapped".

The *EXC-1553PCI/MCH* board contains sets of Jumper arrays that control the 1553 interface (Direct/Transformer Coupled) and a Jumper that controls the Shield Signal.

7.4.1 Channel 0 – Channel 3 1553 Coupling Mode Select Jumpers [JP2–JP17]

Each channel can be either direct-coupled or transformer-coupled to the 1553 bus. Groups of four Jumpers select the coupling mode for each channel.

Table 7-1 defines the Jumper settings for all 16 Jumpers.

Coupling Mode	Setting
Direct-Coupled	Short pins 2 and 3 of channel *[0 – 3]* jumper group
Transformer-Coupled	Short pins 1 and 2 of channel *[0 – 3]* jumper group

Table 7-1 Jumper Settings Required to Select Coupling Mode

Table 7-2 defines the Jumper groups for each channel.

Channel	Bus	Jumper Group
0	A	JP2, JP3
0	B	JP4,JP5
1	A	JP6, JP7
1	B	JP8,JP9
2	A	JP10, JP11
2	B	JP12,JP13
3	A	JP14, JP15
3	B	JP16,JP17

Table 7-2 Channel Jumper Groups

Example: To set channel 0 to transformer-coupled, short with a shorting block, pins 1 and 2, of JP2, JP3, JP4 and JP5.

7.4.2 Factory Default Jumper Settings

The factory default settings are:

JP2–JP17 Pins 1 & 2 Shorted Transformer coupled mode

7.5 Connectors

The *EXC-1553PCI/MCH* and the *EXC-1553cPCI/MCH* each contain two connectors:

1. A female, high-density DB-62 pin connector (J1) [P/N: HDL-62SLC PCB] that contains all the communications signals required for the four channels. (Mating connectors [P/N: HDT 62-DB] with plastic hoods are included. The connector pinouts and signals are described in sections 7.5.1 and 7.5.2.
2. *EXC-1553PCI/MCH*
   PCI Bus Edge Connector. The connector pinouts and signals are described in section **7.5.3 PCI Bus Edge Connector Pinouts**, on page 7-11.
   Or
   EXC-1553cPCI/MCH
   Compact PCI Bus Connector. The connector pinouts and signals are described in section **7.5.4 cPCI Bus Connector Pinouts**, on page 7-12.

7.5.1 Connector J1 Pinouts

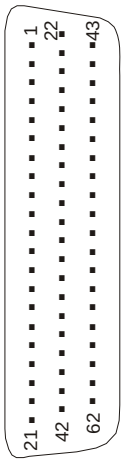


Figure 7-4 Connector J1 – Front View

1	BUSAL0	**22**	SHIELD	**43**	BUSAL1
2	BUSAH0	**23**	SHIELD	**44**	BUSAH1
3	BUSBL0	**24**	SHIELD	**45**	BUSBL1
4	BUSBH0	**25**	SHIELD	**46**	BUSBH1
5	N/C	**26**	GND	**47**	N/C
6	BUSAL2	**27**	SHIELD	**48**	BUSAL3
7	BUSAH2	**28**	SHIELD	**49**	BUSAH3
8	BUSBL2	**29**	SHIELD	**50**	BUSBL3
9	BUSBH2	**30**	SHIELD	**51**	BUSBH3
10	N/C	**31**	SHIELD	**52**	N/C
11	N/C	**32**	GND	**53**	N/C
12	N/C	**33**	SHIELD	**54**	N/C
13	N/C	**34**	SHIELD	**55**	N/C
14	N/C	**35**	SHIELD	**56**	N/C
15	N/C	**36**	SHIELD	**57**	N/C
16	N/C	**37**	GND	**58**	N/C
17	EXTTCLKI	**38**	N/C	**59**	EXTTCLKO
18	N/C	**39**	N/C	**60**	N/C
19	N/C	**40**	N/C	**61**	N/C
20	N/C	**41**	N/C	**62**	N/C
21	N/C	**42**	GND		

Table 7-3 Connector J1 Pinouts

N/C = not connected

7.5.2 Communication I/O Signals Description of Connector J1

Signal	Description
BUSAH0 BUSAL0	Channel #0, Bus A, high connection Channel #0, Bus A, low connection
BUSBH0 BUSBL0	Channel #0, Bus B, high connection Channel #0, Bus B, low connection
BUSAH1 BUSAL1	Channel #1, Bus A, high connection Channel #1, Bus A, low connection
BUSBH1 BUSBL1	Channel #1, Bus B, high connection Channel #1, Bus B, low connection
BUSAH2 BUSAL2	Channel #2, Bus A, high connection Channel #2, Bus A, low connection
BUSBH2 BUSBL2	Channel #2, Bus B, high connection Channel #2, Bus B, low connection
BUSAH3 BUSAL3	Channel #3, Bus A, high connection Channel #3, Bus A, low connection
BUSBH3 BUSBL3	Channel #3, Bus B, high connection Channel #3, Bus B, low connection
SHIELD (case)	Provided for 1553 cables shield connection. This signal is connected to the case of the computer.
EXTTCLKI	External Timer Clock Source Input – required value: 1 MHz This signal supplies an external global clock to all of the channels. It provides the basis for the External Timer Clock (see section 2.4.1 **Channel External Timer Clock Register**, on page 2-11). Use this signal to synchronize the External Timer Clocks on the channels to other boards or systems. [a] See section 2.5.6 **External Timer Clock Source Register**, on page 2-14.
EXTTCLKO	External Timer Clock Source Output (1 MHz). This is the global clock that is supplied to all the channels that forms the basis for their External Timer Clock (see section 2.4.1 **Channel External Timer Clock Register**, on page 2-11). Use this signal to synchronize other boards or systems to the External Timer Clock. [a] The source of this clock is either the External Timer Clock Source Input EXTTCLKI or the Internal Clock Source. See section 2.5.6 **External Timer Clock Source Register**, on page 2-14.
GND	Provides ground reference for the digital signal connections

Table 7-4 Communication I/O Signals Descriptions of Connector J1

a. To Synchronize with External Sources
To synchronize a single *EXC-1553PCI/MCH* board to an external system, the external clock source must be connected to the **EXTTCLKI** signal. See Figure 7-5.

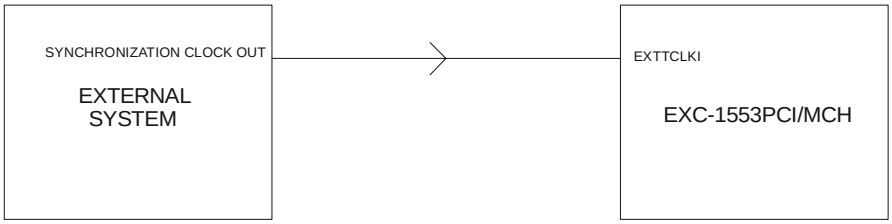


Figure 7-5 Synchronization of a single *EXC-1553PCI/MCH* to an external system

To synchronize an external system to a single *EXC-1553PCI/MCH* board, the EXTTCKLO signal needs to be connected to the external clock source.

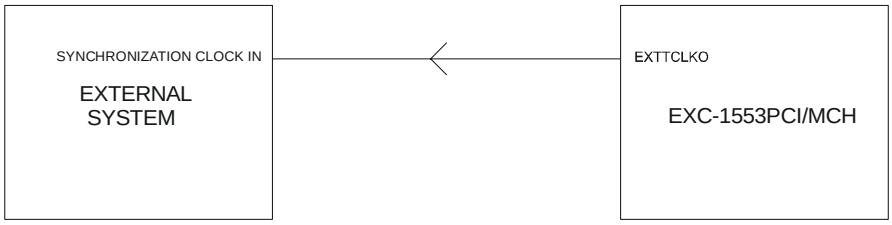


Figure 7-6 Synchronization of an external system to a single *EXC-1553PCI/MCH*

Note The synchronization clock signal may be connected to multiple targets to achieve system wide synchronization.

To Synchronize Between *EXC-1553PCI/MCH* Boards

To synchronize multiple *EXC-1553PCI/MCH* boards the EXTTCLKO signal of one board needs to be connected to all the EXTTCLKI signals of the remaining boards.

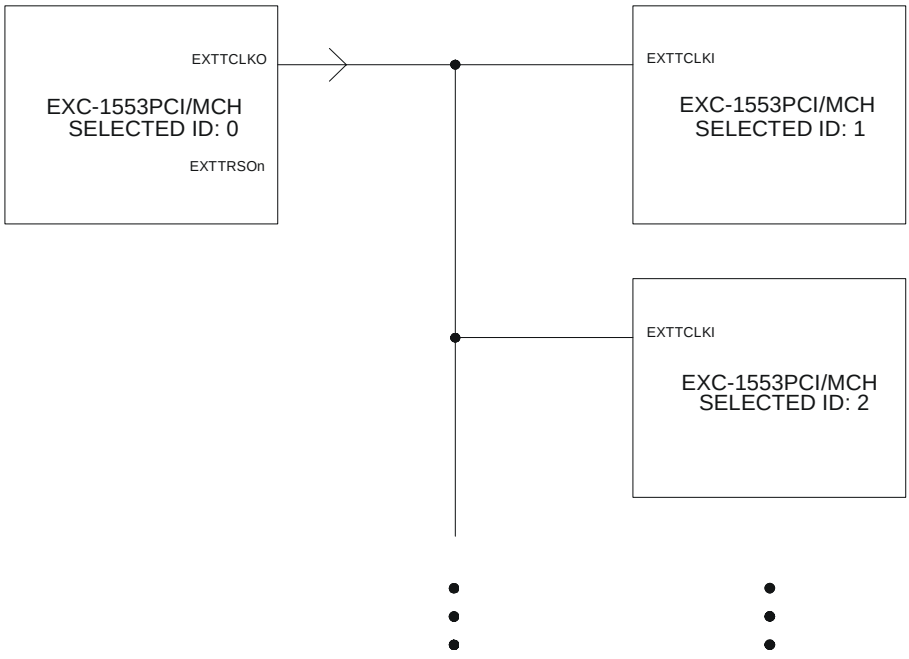


Figure 7-7 Synchronization Between *EXC-1553PCI/MCH* Boards

7.5.3 PCI Bus Edge Connector Pinouts

Pin	PCI Names	Board Signal Names
B1	-12V	-12V
B2	TCK	
B3	GROUND	GND
B4	TDO	
B5	+5V	VCC
B6	+5V	VCC
B7	INTB#	
B8	INTD#	
B9	PRSNT1#	GND
B10	RESERVED	
B11	PRSNT2#	
B12 B13	CONNECTOR KEY	
B14	RESERVED	
B15	GROUND	GND
B16	CLK	CLK
B17	GROUND	GND
B18	REQ#	REQn
B19	+5V (I/O)	
B20	AD[31]	AD31
B21	AD[29]	AD29
B22	GROUND	GND
B23	AD[27]	AD27
B24	AD[25]	AD25
B25	+3.3V	+3.3V
B26	C/BE[3]#	C_BE3n
B27	AD[23]	AD23
B28	GROUND	GND
B29	AD[21]	AD21
B30	AD[19]	AD19
B31	+3.3V	+3.3V
B32	AD[17]	AD17
B33	C/BE[2]#	C_BE2n
B34	GROUND	GND
B35	IRDY#	IRDYn
B36	+3.3V	+3.3V
B37	DEVSEL#	DEVSELn
B38	GROUND	GND
B39	LOCK#	LOCKn
B40	PERR#	PERRn
B41	+3.3V	+3.3V
B42	SERR#	SERRn
B43	+3.3v	+3.3V
B44	C/BE[1]#	C_BE1n
B45	AD[14]	AD14
B46	GROUND	GND
B47	AD[12]	AD12
B48	AD[10]	AD10
B49	GROUND	GND
B50 B51	CONNECTOR KEY	
B52	AD[08]	AD8
B53	AD[07]	AD7
B54	+3.3V	+3.3V
B55	AD[05]	AD5
B56	AD[03]	AD3
B57	GROUND	GND
B58	AD[01]	AD1
B59	+5V (I/O)	
B60	ACK64#	
B61	+5V	VCC
B62	+5V	VCC

Pin	PCI Names	Board Signal Names
A1	TRST#	
A2	+12V	+12V
A3	TMS	
A4	TDI	
A5	+5V	VCC
A6	INTA#	INTAn
A7	INTC#	
A8	+5V	VCC
A9	RESERVED	
A10	+5V	
A11	RESERVED	
A12 A13	CONNECTOR KEY	
A14	RESERVED	
A15	RST#	RSTn
A16	+5V	
A17	GNT#	GNTn
A18	GROUND	GND
A19	RESERVED	
A20	AD[30]	AD30
A21	+3.3V	+3.3V
A22	AD[28]	AD28
A23	AD[26]	AD26
A24	GROUND	GND
A25	AD[24]	AD24
A26	IDSEL	IDSEL
A27	+3.3V	+3.3V
A28	AD[22]	AD22
A29	AD[20]	AD20
A30	GROUND	GND
A31	AD[18]	AD18
A32	AD[16]	AD16
A33	+3.3V	+3.3V
A34	FRAME#	FRAMEn
A35	GROUND	GND
A36	TRDY#	TRDYn
A37	GROUND	GND
A38	STOP#	STOPn
A39	+3.3V	+3.3V
A40	SDONE	
A41	SBO#	
A42	GROUND	GND
A43	PAR	PAR
A44	AD[15]	AD15
A45	+3.3V	+3.3V
A46	AD[13]	AD13
A47	AD[11]	AD11
A48	GROUND	GND
A49	AD[09]	AD9
A50 A51	CONNECTOR KEY	
A52	C/BE[0]#	C_BE0n
A53	+3.3V	+3.3V
A54	AD[06]	AD6
A55	AD[04]	AD4
A56	GROUND	GND
A57	AD[02]	AD2
A58	AD[00]	AD0
A59	+5V	
A60	REQ64#	
A61	+5V	VCC
A62	+5V	VCC

Table 7-5 PCI Bus Edge Connector Pinouts

7.5.4 cPCI Bus Connector Pinouts

25	+5V	N/C	N/C	+3.3V	+5V	GND
24	AD[1]	+5V	N/C	AD[0]	N/C	GND
23	+3.3V	AD[4]	AD[3]	+5V	AD[2]	GND
22	AD[7]	GND	+3.3V	AD[6]	AD[5]	GND
21	+3.3V	AD[9]	AD[8]	N/C	C/BE[0]#	GND
20	AD[12]	GND	N/C	AD[11]	AD[10]	GND
19	+3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	+3.3V	PAR	C/BE[1]#	GND
17	+3.3V	N/C	N/C	GND	PERR#	GND
16	DEVSEL#	GND	N/C	STOP#	LOCK#	GND
15	+3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12–14	KEY AREA					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	+3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	N/C	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	N/C	GND	+3.3V	CLK	AD[31]	GND
5	N/C	N/C	RST#	GND	N/C	GND
4	N/C	GND	N/C	N/C	N/C	GND
3	INTA#	N/C	N/C	+5V	N/C	GND
2	N/C	+5V	N/C	N/C	N/C	GND
1	+5V	–12V	N/C	N/C	+5V	GND
PIN	**A**	**B**	**C**	**D**	**E**	**F**

Table 7-6 cPCI Bus Connector Pinouts

7.6 Power Requirements

The power requirements for each channel installed on the *EXC-1553PCI/MCH* board is:

+5V @ 200mA (0% duty cycle: non-transmitting on 1553 bus)

+5V @ 400mA (25% duty cycle: transmitting on 1553 bus)

+5V @ 560mA (50% duty cycle: transmitting on 1553 bus)

+5V @ 800mA (87.5% duty cycle: transmitting on 1553 bus)

Example: The maximum power requirements for a 2 channels installed (@ 25% duty cycle per channel) will be:

+5V @400mA x 2 = 800mA

8 Ordering Information

The *EXC-1553PCI/MCH* and *EXC-1553cPCI/MCH* are available in one, two, three or four channel versions. When ordering the board indicate the number of channels you require.

The following suffixes must be added to the name of the board to indicate the specific options. The suffixes must be added tot he *EXC-1553PCI/MCH* or *EXC-1553cPCI/MCH* in the order in which they appear in the table.

Suffix	Description
x	Number of channels: 1 – 4
E	Ruggedized, extended temperature option (-40°– +85°C)

ORDERING EXAMPLES:

Part Number	Description
EXC-1553PCI//MCH-1	Single channel, MIL-STD-1553, interface board for PCI systems. Supports BC, RT, RT/Concurrent-BM and BM modes.
EXC-1553cPCI/MCH-2	Dual channel, MIL-STD-1553interface board for compact PCI systems. Supports BC, RT, RT/Concurrent-BM and BM modes.
EXC-1553cPCI/MCH-2-E	Same as above with ruggedized, extended temperature option (-40°– +85°C)
EXC-1553PCI/MCH-3	Three channel, MIL-STD-1553, interface board for PCI systems. Supports BC, RT, RT/Concurrent-BM and BM modes.
EXC-1553cPCI/MCH-4	Four channel, MIL-STD-1553 interface board for compact PCI systems. Supports BC, RT, RT/Concurrent-BM and BM modes.
EXC-1553cPCI/MCH-4-E	Same as above with ruggedized, extended temperature option (-40°– +85°C)

Appendix A MIL-STD-1553 Word Formats

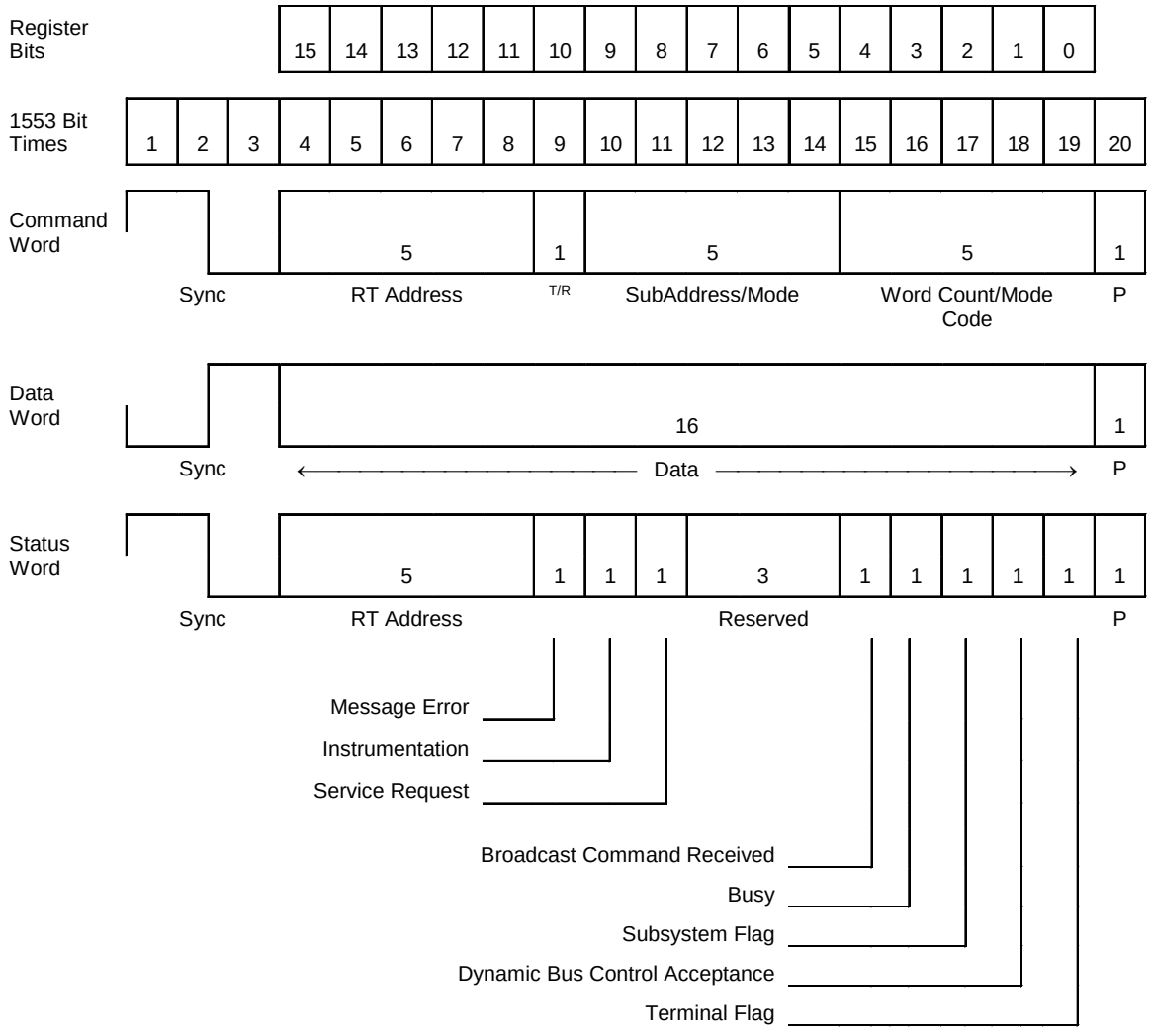


Figure A-1 MIL-STD-1553 Word Formats

Note: T/R = Transmit/Receive
P = Parity

Appendix B MIL-STD-1553 Message Formats

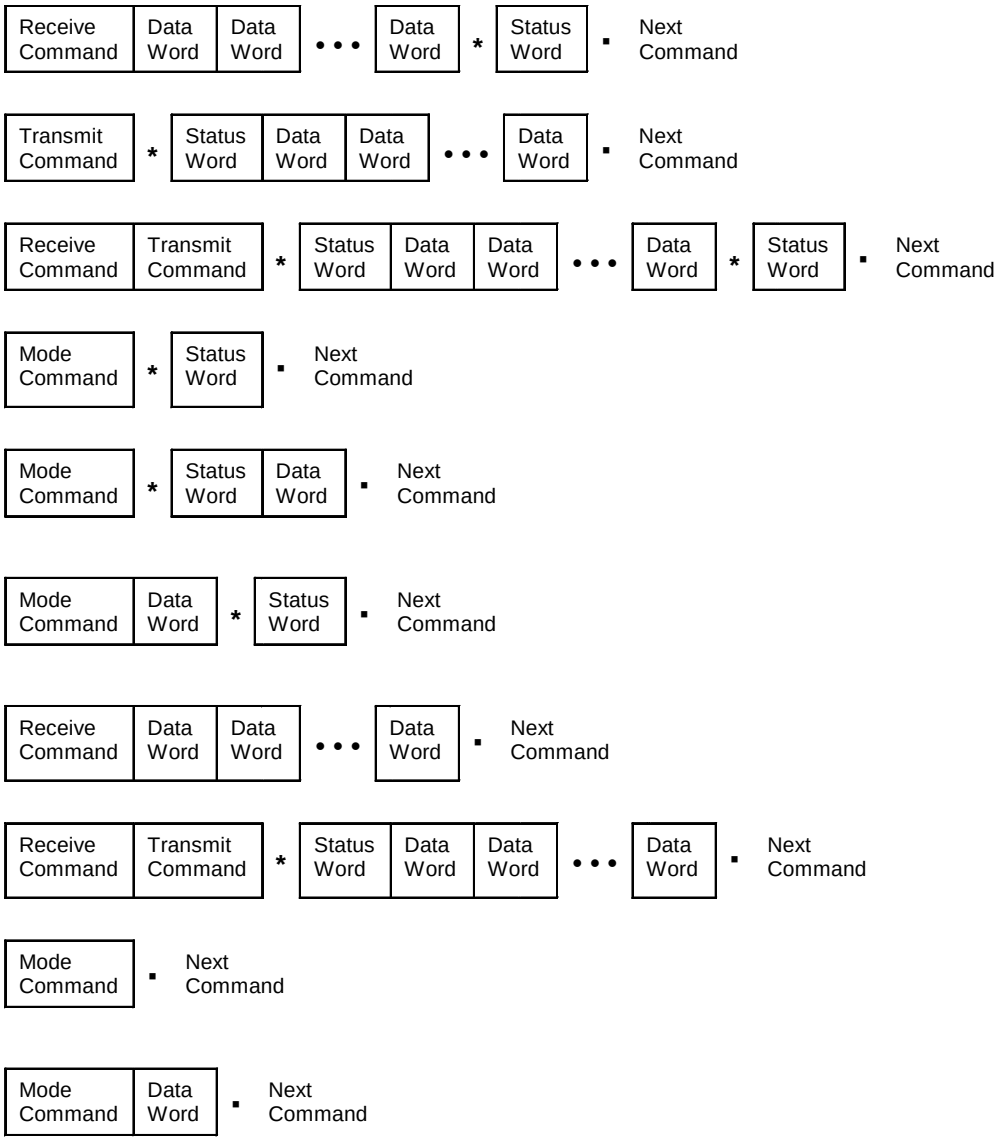


Figure B-1 MIL-STD-1553 Message Formats

Note: * = Response time
▪ = Intermessage Gap

The information contained in this document is believed to be accurate. However, no responsibility is assumed by Excalibur Systems, Inc. for its use and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

December 2007, Rev A-4